

# ESDA/JEDEC Joint Standard

**ANSI/ESDA/JEDEC JS-001-2023**

Revision of ANSI/ESDA/JEDEC JS-001-2017



*For Electrostatic Discharge  
Sensitivity Testing*

*Human Body Model (HBM)  
Device Level*

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Electrostatic Discharge  
Sensitivity Testing***

***Human Body Model (HBM)  
Device Level***

Approved

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## FOREWORD

This joint standard was developed under the guidance of the JEDEC JC-14.1 committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The original content for the initial version (2010) was developed by a joint working group composed of members of the JEDEC ESD Task Group and ESDA Working Group 5.1 (Human Body Model). This version of the standard is intended to replace the human body model ESD standard ANSI/ESDA/JEDEC JS-001-2017.

The purpose has been modified to allow testing at package, wafer, or die level with a warning that results may be different.

Definitions have been improved or added to specify better HBM simulator definition and its parts (like terminal, channel, pin), no-connect pins, and exposed pads.

Low parasitic tester definition has been improved, specifying that the possibility of using a low parasitic system depends on the number of channels that meet waveform requirements; this also includes two-channel testers.

Text in several subsections of Section 6.0 has been revised to clarify the “equivalence” of using Table 2A, Table 2B, and pin-pair stressing and to specify that it is required to complete full pin to pin stress on a device having 10 pins or less, but it is allowed to use the same strategy on a device having a higher pin count. A reference for assigning withstand thresholds to a subset of pins has been included in the same section with more detail in Annex B.

The compendium for this document is ESDA/JEDEC JTR001, where legacy JS-001-2017 annexes C and D have been moved and expanded together with suggestions and other practical examples for helping the interpretation of this norm.

Minor changes include modifications in Table 1, Table 2A, and Table 2B, reference to JTR001 where appropriate, annex reordering, and editorial changes in the body and the images.

In this document, the following verbal forms are used:

- “shall” indicates a requirement
- “should” indicates a recommendation
- “may” indicates a permission
- “can” indicates a possibility or a capability

This standard is maintained and revised as a joint standard through a Memorandum of Understanding between JEDEC and ESDA. This standard is a living document. Revisions and updates will be made on a routine basis, driven by the needs of the electronic industry.

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**ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Device Level****1.0 SCOPE AND PURPOSE****1.1 Scope**

This standard establishes the procedure for testing, evaluating, and classifying devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

All packaged semiconductor devices, thin film circuits, acoustic wave devices, optoelectronic devices, hybrid integrated circuits (HICs), discrete, and multi-chip modules (MCMs) containing any of these devices as well as unpackaged singulated bare die, and die which are still part of a wafer are to be evaluated according to this standard.

**1.2 Purpose**

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

**1.3 Equivalency of Wafer or Die Level Results**

HBM test results at the wafer or die level are considered valid and equivalent but may differ from testing in a package due to package parasitics, pins tied together in the package, or any other devices included in the package.

**2.0 REFERENCED PUBLICATIONS**

ESD ADV1.0, ESD Association's Glossary of Terms<sup>1</sup>

JESD99, JEDEC Standard - Terms, Definitions, and Letter Symbols for Microelectronic Devices<sup>2</sup>

ESDA/JEDEC JTR001-xx-xx, User Guide of ANSI/ESDA/JEDEC JS-001 Human Body Model Testing of Integrated Circuits

**3.0 DEFINITIONS**

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms, and JESD99 JEDEC Standard –Terms, Definitions, and Letter Symbols for Microelectronic Devices. Terms separated by a semicolon (;) are considered to be synonyms. In this document, the term “pin” is used to represent any device pin, land, bump, ball, or die pad.

**above-passivation layer (APL).** A low-impedance metal plane built on the surface of a die above the passivation layer connecting a group of bumps or pins (typically power or ground).

NOTE: This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs (sometimes referred to as islands) for a power or ground group.

**associated non-supply pin.** A non-supply pin (typically an input, output, or I/O pin) is associated with a supply pin group if either:

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- the current from the supply pin group (for example, VDDIO) is required for the function of an electrical circuit (I/O driver) that connects (high/low impedance) to that non-supply pin; or
- a parasitic path exists between a non-supply and supply pin group (for example, open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

**cloned non-supply (IO) pin.** Any of a set of input, output, or bidirectional pins using the same IO cell and electrical schematic and sharing the same associated supply pin group(s), including ESD power clamp(s).

**coupled non-supply pin pair.** Two pins, such as differential amplifier inputs or low-voltage differential signaling (LVDS) pins, having an intended direct current path in between, such as a pass gate or resistor.

NOTE: These pairs include analog and digital differential pairs and other special function pairs (for example, D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP\_DP/CCN\_DN, etc.).

**ESD withstand voltage; withstand threshold.** The highest voltage level not causing device failure with the device passing all tests performed at lower voltage levels.

NOTE: See note under “failure window” definition.

**exposed pad.** An exposed metal plate on an IC package.

NOTE: This metal plate may or may not be electrically connected to the die.

NOTE: If the exposed pad supports the die, it might be called a die attach pad or thermal pad (see ESDA/JEDEC JTR001 for further information).

**failure window.** An intermediate range of stress conditions inducing failure in a particular device type while the device type can pass some higher and lower stress conditions than this range.

NOTE: For example, a device with a failure window may pass a 500-volt test, fail a 1000-volt test, and pass a 2000-volt test. Hence, the failure window of the device is between 500 volts and 2000 volts. The withstand voltage of this device is 500 volts, as this is the highest passing level before the 1kV failure.

**feedthrough.** A direct or indirect (via a series resistor) connection from a pad cell layout allowing additional elements not included in the pad cell to make electrical connections to the bond pad (see Annex A).

**HBM ESD tester; HBM simulator.** Equipment that applies a simulated human body model (HBM) ESD stress to a device.

**human body model (HBM) ESD.** An electrostatic discharge (ESD) event meeting the waveform criteria specified in this standard approximating the discharge from the fingertip of a typical human being to a grounded device.

**Ips (peak current value).** The current value determined by linear extrapolation of the exponential current decay curve back to the time ( $t_{max}$ ) when the current actually peaked ( $Ips_{max}$ ).

NOTE: The linear extrapolation should be based on the current waveform data over a 40-nanosecond period beginning at  $t_{max}$  (see Figure 2A).

**Ips<sub>max</sub> (peak current maximum value).** The highest current value measured.

NOTE: This value includes the overshoot or ringing components due to internal test simulator RLC parasitics (see Figure 2A).

**N-channel low parasitic HBM simulator.** A simulator with similar in-specification waveforms for both polarities and terminal A/B orientations when performing the procedure in Section 5.2.2 on a pair of pins formed by a single pin and one pin of a pin group with N pins connected to N channels of the tester.

**no-connect pin.** A package interconnect (pin, bump, or ball) not electrically connected to a die.

NOTE: In practice, some pins are labeled as “no-connect” but are actually connected to the die and, therefore, should not be classified as no-connect pins for ESD testing.

**non-socketed tester.** An HBM simulator making contact with the device under test (DUT) pins (or balls, lands, bumps, or die pads) with test probes rather than placing the DUT in a socket.

**non-supply pin.** A pin that is not categorized as a supply pin or a no-connect.

NOTE: Non-supply pins include pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins, and VPP pins on EPROM memory. Most non-supply pins transmit or receive information, such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

**package plane.** A low-impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground). There may be multiple package planes (sometimes referred to as islands) for each power and ground group.

**pin.** Any terminal, land, lead, bump, ball, or exposed pad on the package that may make an electrical connection to the die.

**pre-pulse voltage.** A voltage occurring at the device under test (DUT) immediately prior to the generation of the HBM current pulse (see Annex C.2).

**pulse generation circuit.** The circuit network that produces a human body discharge current waveform.

NOTE: The circuit network includes a pulse generator with its test equipment internal path up to the contact pad of the test fixture.

NOTE: This circuit is also referred to as a dual-polarity pulse source.

**ringing.** A high-frequency oscillation superimposed on a waveform.

**shorted non-supply pin.** Any non-supply pin (typically an input, output, or I/O pin) that is metallically connected (typically < 3 ohms) on the chip or within the package to another non-supply pin (or set of non-supply pins).

**socketed tester.** A simulator that makes contact with DUT pins (or balls, lands, bumps, or die pads) using a DUT socket mounted on a test fixture board.

**specification limit (SPL).** The HBM limit value set by customer requirements or internal targets (see Annex A).

**spurious current pulse.** A small HBM shaped pulse following the main current pulse, typically defined as a percentage of  $I_{ps_{max}}$ .

**step-stress-test hardening.** The process of increasing the ESD withstand threshold by applying stress incrementally from low voltage to higher values.

NOTE: This hardening occurs when a device subjected to increasing ESD voltage step-stresses can withstand higher stress levels than when another device expected to have the same threshold is evaluated using no step-stressing.

NOTE: For example, a device may fail at 1000 volts if subjected to a single stress but fail at 3000 volts if stressed incrementally from 250 volts.

**supply pin.** Any device pin that provides an operating current to that device.

NOTE: Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current reference levels). For ESD testing, power and ground pins are treated as supply pins.

**terminal.** Output (A) or return (B) of the simulator pulse source.

**test fixture board.** A specialized circuit board with one or more device sockets connecting the DUT(s) to the HBM simulator.

**tester channel.** A path connecting the pulse source of the simulator to the DUT pin.

**$t_{max}$ .** The time when the current is at its maximum value ( $I_{ps_{max}}$ ) (see Figure 2A).

**trailing current pulse.** A current pulse that occurs after the HBM current pulse has decayed (see Annex C.1).

NOTE: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

**two-channel tester.** An HBM simulator that has two tester channels.

**V1.** The minimum HBM stress voltage step at which at least one of the selected cloned non-supply pins fails (see Annex A).

**V2.** The estimation of the minimum HBM stress voltage step at which all selected cloned non-supply pins would fail (see Annex A).

**VM.** The minimum HBM stress voltage step at which 50% or greater of the selected cloned non-supply pins fail (see Annex A).

## 4.0 APPARATUS AND REQUIRED EQUIPMENT

### 4.1 Waveform Verification Equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current probe, and high-voltage resistor load. The maximum time between calibrations shall be according to company quality management system requirements.

Equipment capable of verifying the pulse waveforms defined in this standard test method includes but is not limited to, an oscilloscope, evaluation loads, and a current probe.

#### 4.1.1 Oscilloscope

A digital oscilloscope is recommended, but analog oscilloscopes are also permitted. The oscilloscope shall meet the following requirements to ensure accurate current waveform capture:

- a. Minimum sensitivity of 100 milliamperes per major division when used in conjunction with the current probe specified in Section 4.1.2.
- b. Minimum bandwidth of 350 MHz.
- c. Recommended minimum channels: 2
- d. Minimum vertical accuracy: + 2.5%
- e. Minimum time base accuracy: 0.01%
- f. For analog scopes, the minimum writing rate of one major division per nanosecond.

##### 4.1.1.1 Additional Requirements for Digital Oscilloscopes

- a. Minimum sampling rate: 1 GS/s
- b. Minimum vertical resolution: 8-bit
- c. Minimum record length: 10 k points

#### 4.1.2 Current Probe

- a. Minimum bandwidth of 200 MHz
- b. Minimum peak pulse capability of 8 amperes
- c. Rise time of less than 1 nanosecond
- d. Capable of accepting a solid conductor as specified in Section 4.1.3.
- e. Provides an output voltage per signal current as required in Section 4.1.1. (This is usually between 1 and 5 millivolts per milliampere).
- f. Low-frequency 3-dB-point below 10 kHz (for example, Tektronix CT2) for measurement of the decay constant  $t_d$  (see Section 5.2.3.1, Table 1, and note below).

NOTE: Results using a current probe with a low-frequency 3-dB-point of 25 kHz (for example, Tektronix CT1) to measure decay constant  $t_d$  are acceptable if  $t_d$  is found to be between 130 and 165 nanoseconds.

#### 4.1.3 Evaluation Loads

Two evaluation loads are necessary to verify tester functionality:

- a. Load 1: A solid 18-24 AWG (non-US standard wire size 0.25 to 0.75 mm<sup>2</sup> cross-section) tinned copper wire (shorting load) as short as practical to span the distance between the two farthest pins in the socket contacted by the probes of a non-socketed tester. The wire should be long enough to pass through the current probe.
- b. Load 2: 500 ohms,  $\pm 1\%$ , minimum 4000-volt rating.

#### 4.1.4 Attenuator

A 20.0-dB attenuator with a precision of  $\pm 0.5$  dB, at least 1-GHz bandwidth, and an impedance of 50 ohms  $\pm 5$  ohms.

## 4.2 Human Body Model Simulator

A simplified schematic of the HBM simulator or tester is given in Figure 1. The performance of the tester is influenced by parasitic capacitance and inductance. Thus, the construction of a tester using this schematic does not guarantee that it will provide the HBM pulse required for this standard. The waveform capture procedures and requirements described in Section 5.0 determine the acceptability of the equipment for use.

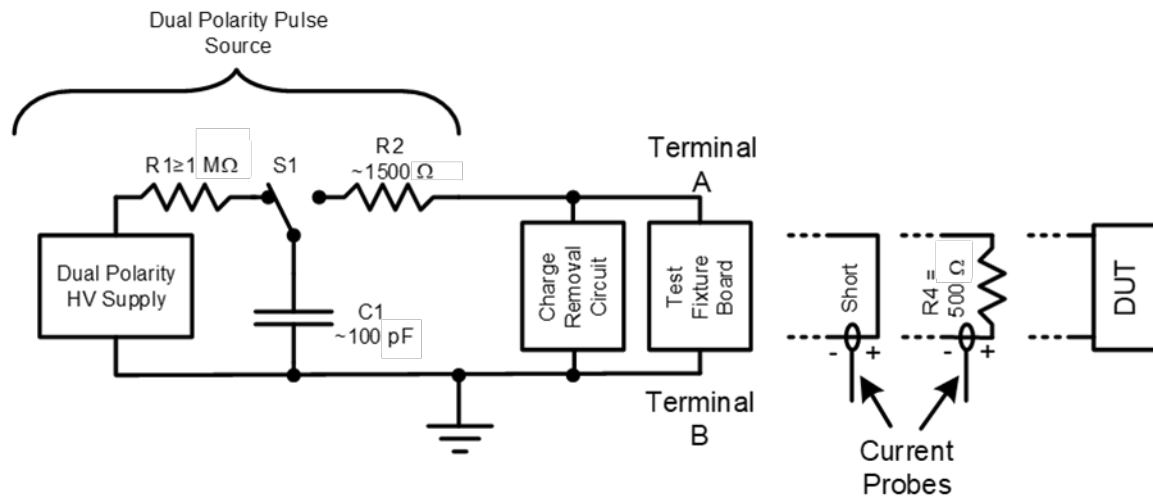


Figure 1: Simplified HBM Simulator Circuit with Loads

#### NOTES:

1. The current probes are specified in Section 4.1.2.
2. The shorting load (Short) and 500-ohm resistor (R4) are evaluation loads specified in Section 4.1.3.
3. Reversal of Terminals A and B to achieve dual-polarity performance is not permitted except under conditions described in, Sections 6.5.1.3 and 6.7.
4. The charge removal circuit ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge. A simple example is a 10-kilohm or larger resistor (possibly in series with a switch) in parallel with the test fixture board. This resistor may also be useful to control parasitic pre-pulse voltages (see Annex C.2 and Annex C.3).
5. The dual polarity pulse source (generator) shall be designed to avoid recharge transients and double pulses.
6. Stacking of DUT socket adapters (piggybacking or the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard defined in Table 1.
7. Values in this figure are nominal.

#### 4.2.1 HBM Test Equipment Parasitic Properties

Some HBM simulators have been found to incorrectly classify HBM sensitivity levels due to parasitic artifacts or uncontrolled voltages unintentionally built into the HBM simulator's environment. Annex C describes methods for determining if these effects are present and optional mitigation techniques. See Annex C.5 for a procedure to determine if an HBM simulator is

considered an N-channel low-parasitic HBM simulator for a device with N pins simultaneously connected to the simulator.

## 5.0 STRESS TEST EQUIPMENT QUALIFICATION AND ROUTINE VERIFICATION

### 5.1 Overview of Required HBM Tester Evaluations

The HBM tester and test fixture boards shall be qualified, re-qualified, and periodically verified as described in this section. A flow chart for this procedure is given in Annex D. The safety precautions described in Section 5.8 should be followed at all times.

### 5.2 Measurement Procedures

#### 5.2.1 Reference Pin Pair Determination

The two pins of each socket on a test fixture board that make up the reference pin pair are:

1. The socket pin with the shortest wiring path of the test fixture to the pulse generation circuit (Terminal B).
2. The socket pin with the longest wiring path of the test fixture from the pulse generation circuit (Terminal A) to the ESD stress socket (see Figure 1).

This information is typically provided by the equipment or test fixture board manufacturer. If more than one pulse generation circuit is connected to a socket, there will be more than one reference pin pair.

It is strongly recommended that on non-positive clamp fixtures, feed through test point pads be added on these paths to connect either the shorting load or 500-ohm load resistor during waveform verification measurements. These test points should be added as close as possible to the socket(s), and if the test fixture board uses more than one pulse generator, multiple feed through test points should be added for each pulse generator's longest and shortest paths.

NOTE: A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting load to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

#### 5.2.2 Waveform Capture with Current Probe

To capture a current waveform between two socket pins (usually the reference pin pair), use the shorting load (see Section 4.1.3, Load 1) for the short-circuit measurement or the 500-ohm resistor (see Section 4.1.3, Load 2) for the 500-ohm current measurement and the current probe (see Section 4.1.2).

NOTE: At high stress voltages, an attenuator (see Section 4.1.4) may be necessary to prevent off-scale measurements on the oscilloscope and avoid oscilloscope damage. At low stress levels, especially at the 50-volt and 125-volt levels, an attenuator should not be used when signal levels reach the lower limits of the oscilloscope voltage sensitivity.

##### 5.2.2.1 Short-Circuit Current Waveform

Place the current probe around the shorting load, as close to Terminal B as practical, observing the polarity shown in Figure 1. Attach the shorting load between the pins to be measured, with the current probe as close to Terminal B as practical, observing the polarity shown in Figure 1. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification, or periodic verification.

- a. For positive clamp sockets, insert the shorting load between the socket pins connected to Terminals A and B and hold it in place by closing the clamp.
- b. For non-positive clamp sockets, attach the shorting load between the socket pins connected to Terminals A and B. If it is not possible to make contact within the socket, connect the shorting load between the reference pin pair feed through test points, if available.

NOTE: The socket design is important as some socket types may include contact springs (coils) in their design. These springs can add more parasitic inductance to the signal path and may affect the HBM



waveform. Selecting sockets that minimize the use of springs (coils) is recommended, but if this is not possible, then keeping their length as short as possible is recommended.

- c. For non-socketed testers, the shorting load with the inductive current probe is placed on an insulating surface, and the simulator Terminal A and Terminal B probes are placed on the ends of the wires.

#### 5.2.2.2 500-Ohm Load Current Waveform

Place the current probe around the 500-ohm resistor's lead, observing the polarity shown in Figure 1. Attach the 500-ohm resistor between the pins to be measured with the current probe as close to Terminal B as practical. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification, or periodic verification.

- a. For socketed testers, follow procedures according to socket type as described in Section 5.2.2.1.
- b. For non-socketed testers, place the test load and current probe on an insulating surface and connect the tester's probes to the ends of the test load.

### 5.2.3 Determination of Waveform Parameters

The captured waveforms are used to determine the parameter values listed in Table 1.

#### 5.2.3.1 Short-Circuit Waveform

Typical short-circuit waveforms are shown in Figures 2A, 2B, and 4. The parameters  $I_{ps}$  (peak current),  $t_r$  (pulse rise time),  $t_d$  (pulse decay time), and  $I_R$  (ringing) are determined from these waveforms. Ringing may prevent the simple determination of  $I_{ps}$ . A graphical technique for determining  $I_{ps}$  and  $I_R$  is described in Section 5.2.3.3 and Figure 4.

#### 5.2.3.2 500-Ohm Load Waveform

A typical 500-ohm load waveform is shown in Figure 3. The parameters  $I_{pr}$  (peak current with 500-ohm load) and  $t_{tr}$  (pulse rise time with 500-ohm load) are determined from this waveform.

#### 5.2.3.3 Graphical Determination of $I_{ps}$ and $I_R$ (see Figure 4)

**5.2.3.3.1** A line is drawn (manually or using numerical methods such as least squares) through the HBM ringing waveform from  $t_{max}$  to  $t_{max} + 40$  ns to interpolate the value of the curve for a more accurate derivation of the peak current value ( $I_{ps}$ ).  $t_{max}$  is the time when  $I_{ps_{max}}$  occurs (see definition for  $t_{max}$  in Section 3 and Figure 2A).

**5.2.3.3.2** The maximum deviation of the measured current above the straight-line fit is Ring1. The maximum deviation of the measured current below the straight-line fit is Ring2. The maximum ringing current during a short-circuit waveform measurement is defined as:

$$I_R = |\text{Ring1}| + |\text{Ring2}|$$

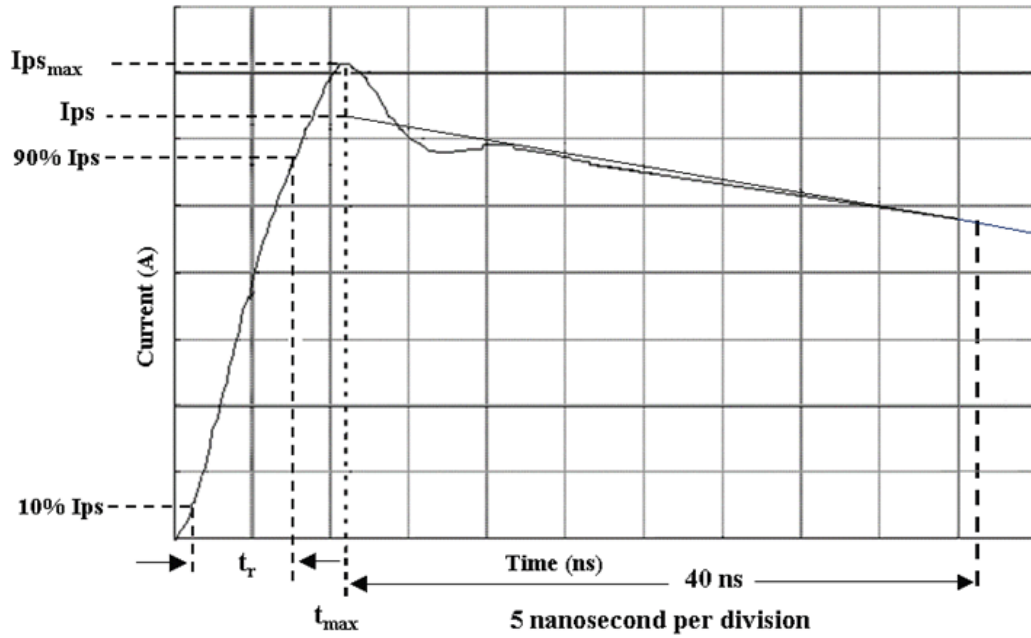


Figure 2A: Current Waveform through a Shorting Load ( $I_{ps\_max}$ )

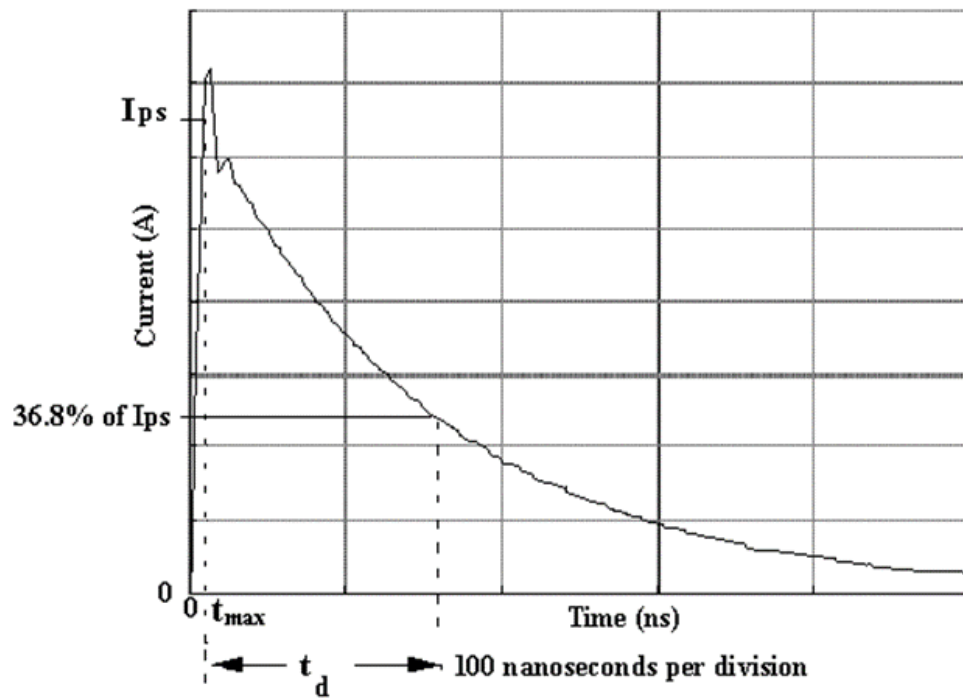


Figure 2B: Current Waveform through a Shorting Load ( $t_d$ )

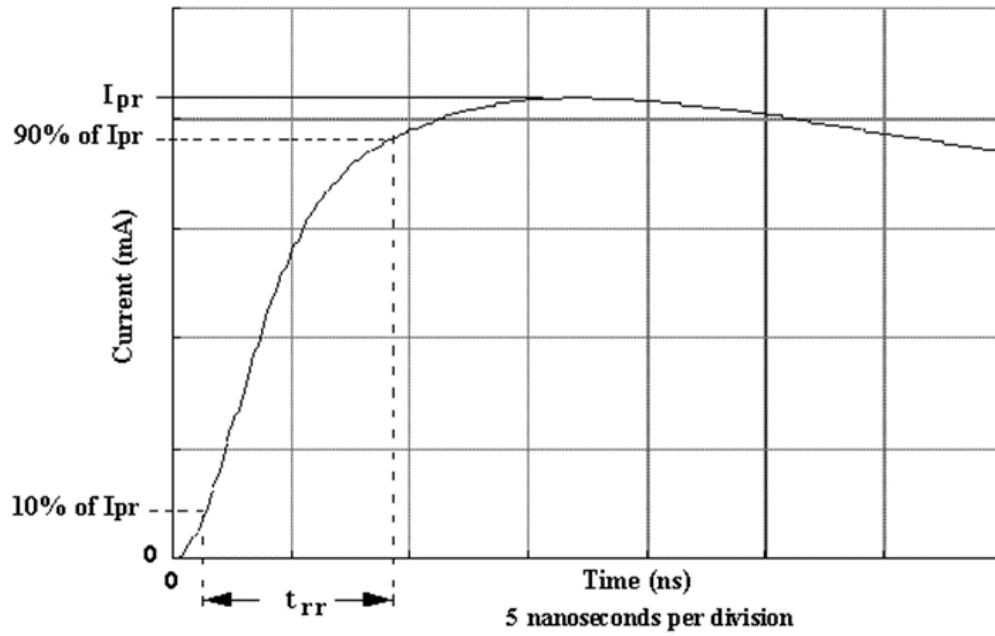


Figure 3: Current Waveform through a 500-ohm Resistor

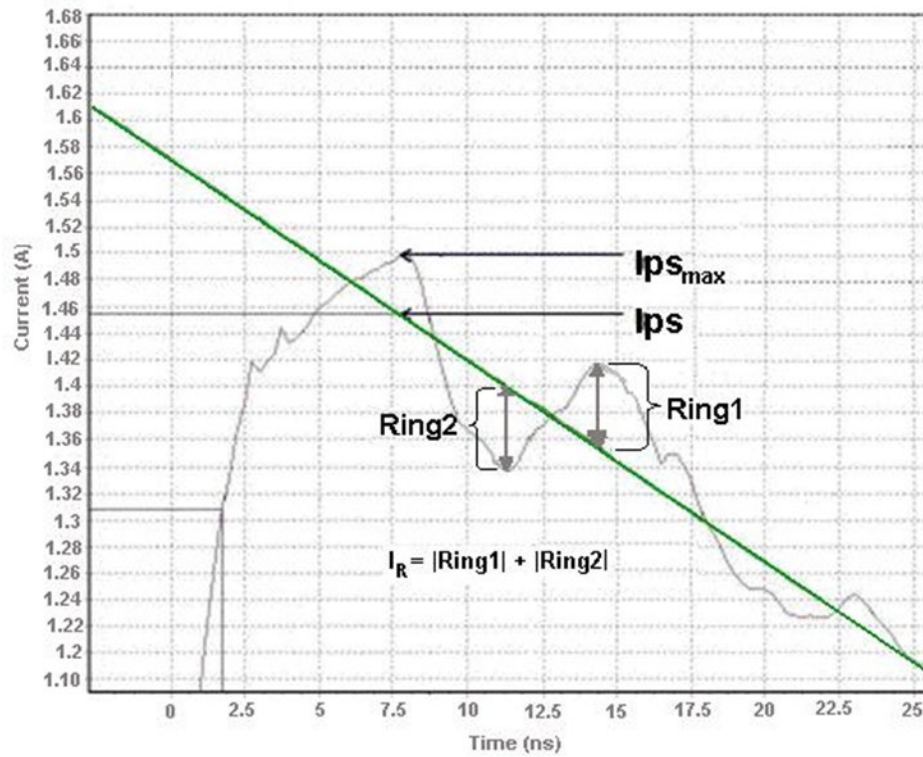


Figure 4: Peak Current Short-Circuit Ringing Waveform

#### **5.2.4 High-Voltage Discharge Path Test**

This test is only required for relay-based testers. This test is intended to ensure that the tester high-voltage relays and the grounding relays that connect pulse generator(s) (that is, Terminal A) and current return paths (that is, Terminal B) to the DUT are functioning properly. The tester manufacturer should provide a recommended procedure and, if needed, a verification board and software.

#### **5.3 HBM Tester Qualification**

HBM ESD tester qualification, as described in this section, is required in the following situations:

- a. Acceptance testing when the ESD tester is delivered or prior to first use.
- b. Periodic re-qualification in accordance with the manufacturer's recommendations. The maximum time between re-qualification tests is one year.
- c. After service or repair that could affect the waveform.

##### **5.3.1 HBM Tester Qualification Procedure**

###### **5.3.1.1 Test Fixture Board, Socket, and Pins for Socketed Testers Only**

Use the highest pin count test fixture board with a positive clamp socket for the tester waveform verification or the recommended waveform verification board provided by the manufacturer.

The reference pin pair(s) of the highest pin count socket on the board shall be used for waveform capture. Waveforms from every pulse generating circuit are to be recorded.

Electrical continuity for all pins on the test fixture board shall be verified prior to qualification testing. This can typically be done using the manufacturer's recommended self-test.

###### **5.3.1.2 Short-Circuit Waveform Capture**

- a. For socketed testers: Configure the test fixture board, shorting load, and current probe for the short-circuit waveform measurement described in Section 5.2.2.1.  
For non-socketed testers: Configure the shorting load and current probe for the short-circuit waveform measurement described in Section 5.2.2.1(c).
- b. Apply five positive and five negative pulses at each non-optional test voltage in Table 1. Verify that the waveforms meet all parameters specified in Figures 2A, 2B, and 4, and Table 1. Record all waveforms.
- c. If the optional levels (50 volts, 125 volts, and/or 8000 volts) are intended to be used, then steps a and b shall be completed for those levels.

###### **5.3.1.3 500-Ohm Load Waveform Capture**

- a. For socketed testers: Configure the test fixture board, resistor, and current probe for the 500-ohm load waveform measurement as described in Section 5.2.2.2.  
For non-socketed testers: Configure the resistor and current probe for the 500-ohm load waveform measurement described in Section 5.2.2.2(b).
- b. Apply and record five waveforms at 1000 volts and 4000 volts, both positive and negative polarities. Verify that the waveforms meet all parameters specified in Figure 3 and Table 1.

###### **5.3.1.4 Spurious Current Pulse Detection**

Secondary pulses after the HBM pulses are generated by the discharge relay. Using the shorting load configuration, initiate a 1000-volt pulse and verify that any pulses after the initial HBM pulse are less than 15% of the amplitude of the main pulse.

NOTE: For analog oscilloscopes, setting the time base to 1 millisecond/division can detect these types of pulses. For digital oscilloscopes, current pulses after the initial current pulse can be observed, but advanced

triggering functions such as sequential triggering or delayed triggering may be needed, so secondary pulses are not missed due to low sampling rates.

#### **5.4 Test Fixture Board Qualification for Socketed Testers**

Test fixture boards shall be qualified in a qualified tester prior to initial use or after repair. This procedure is also required when a previously qualified test fixture board is used in a different model HBM simulator from the one in which it was originally qualified. The procedure shall be applied to the reference pin pairs on all sockets of the new test fixture board. If there is not adequate physical access to the socket, follow the guidance of Section 5.2.2.1(b).

**5.4.1** Configure the test fixture board, shorting load, and current probe for the short-circuit waveform measurement described in Section 5.2.2.1 with a qualified tester.

**5.4.2** Apply at least one positive and one negative 1000-volt pulse. All waveform parameters shall be within the limits specified in Figures 2A, 2B, and 4 and Table 1.

**5.4.3** Configure the test fixture board, 500-ohm resistor, and current probe for the 500-ohm load waveform measurement described in Section 5.2.2.2.

**5.4.4** Apply at least one positive and one negative 1000-volt pulse. All waveform parameters shall be within the limits specified in Figure 3 and Table 1.

**5.4.5** Repeat for all additional reference pin pairs of all pulse generating circuits and sockets.

Table 1. Waveform Specification

Voltage Level (V)	I <sub>peak</sub> for Short, I <sub>ps</sub> (A)	I <sub>peak</sub> for 500 Ω, I <sub>pr</sub> (A)	Rise Time for Short, t <sub>r</sub> (ns)	Rise Time for 500 Ω, t <sub>rr</sub> (ns)	Decay Time for Short, t <sub>d</sub> (ns)	Maximum Ringing Current for Short, I <sub>R</sub> (A)
50 (optional)	0.027-0.040	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
125 (optional)	0.075-0.092	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
250	0.15-0.18	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
500	0.30-0.37	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
1000	0.60-0.73	0.37-0.55	2.0-10	5.0-25	130-170	15% of I <sub>ps</sub>
2000	1.20-1.47	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>
4000	2.40-2.93	1.5-2.2	2.0-10	5.0-25	130-170	15% of I <sub>ps</sub>
8000 (optional)	4.80-5.87	N/A	2.0-10	N/A	130-170	15% of I <sub>ps</sub>

## 5.5 Routine Waveform Check Requirements

### 5.5.1 Standard Routine Waveform Check Description

Waveforms shall be acquired using the short circuit method (see Section 5.2.2.1) on each socket's reference pin pair(s). If necessary, the test fixture board being used may be removed and replaced with a positive clamp socket test fixture board to facilitate waveform measurements. For non-socketed testers, the procedure of Section 5.2.2.1(c) is used. Stresses shall be applied at positive and negative 1000 volts or the stress level tested during the use. The waveforms shall meet the requirements of Figures 2A, 2B, and 4 and Table 1.

#### 5.5.1.1 Waveform Check Frequency

The waveforms shall be verified according to this procedure at least once per shift. If ESD stress testing is performed in consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between waveform checks may be used if no changes in waveforms are observed for several consecutive checks. Simpler waveform checks (see Section 5.5.2) may be used with a longer period between waveform checks, as described in this section. For example, Section 5.5.2 tests may be done daily, with tests according to Section 5.5.1 done monthly. The test frequency and method chosen shall be documented. If at any time the waveforms no longer meet the specified

limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

If the tester has multiple pulse generation circuits, then the waveform for each pulse generation circuit shall be verified with a positive clamp socket test fixture board. The recommended period between verification tests is once per shift. However, a rotational verification method may be used to ensure all pulse generation circuits are functioning properly. For instance, on day 1, the pulse generation circuit 1 would be tested. On day 2, the pulse generation circuit 2 would be tested, and on day 3, the pulse generation circuit 3 would be tested until all circuits have been tested, at which time circuit 1 would again be tested. The recommended maximum interval between tests of any one pulse generator is two weeks. However, if a pulse generation circuit fails, then all ESD stress tests subsequent to the previous satisfactory waveform check of that pulse generation circuit shall be marked invalid and shall not be used for classification.

### **5.5.2 Alternate Routine Waveform Capture Procedure**

As an alternative to the detailed routine waveform analysis, a quick pass/fail waveform capture process can be instituted for routine verification. This method may be used in combination with Section 5.5.1, as described above.

5.5.2.1 Capture a waveform using a shorting load evaluation load at +1000 volts.

5.5.2.2 Measure  $I_{ps_{max}}$  (without adjustment for ringing) and ensure that it is between 0.60 and 0.73 amperes.

5.5.2.3 Repeat at -1000 volts.

5.5.2.4 If the tester has multiple pulse sources, choose a pin pair combination from a different pulse source each day, rotating through each pulse source in turn, as described in Section 5.5.1.1.

If  $I_{ps_{max}}$  is within the values specified for both polarities and the waveforms appear normal, the tester is considered ready to use.

NOTE: This measurement does not take into consideration  $I_{ps}$  ringing; this may affect the results. If there are any concerns about how the waveforms look, or if the measurements are close to the upper or lower specification limits, a complete waveform analysis (Section 5.3.1) shall be performed.

NOTE: The quick pass/fail test method should be applied only to qualified test fixture boards for qualified ESD simulators. Test fixture boards and ESD simulator shall be qualified together using the test method in Section 5.3.1 before using the test method in Section 5.5.2.

## **5.6 High-Voltage Discharge Path Check**

### **5.6.1 Relay Testers**

This test is required for either routine check method (Section 5.5). Test the high-voltage discharge and current return paths and all associated circuitry at the beginning of each day, during which ESD stress testing is performed (see Section 5.2.4). The period between self-test diagnostic checks may be extended, providing test data supports the increased interval. If any failure is detected, do not perform device testing with the sockets connected to the defective discharge paths. Repair the tester and then verify that the failed pins pass the self-test before resuming testing. Depending on the extent of the repair, it may be necessary to perform a complete re-qualification according to Section 5.3.1.

### **5.6.2 Non-Relay Testers**

For testers utilizing mechanical switching instead of relay switching, the connections to pins shall be verified for each pin combination during the test. Making continuity measurements immediately prior to stress pulses or monitoring the HBM pulse current during stress pulses are examples of

connection verification methods. This practice replaces the daily high-voltage discharge path verification.

## **5.7 Tester Waveform Records**

### **5.7.1 Tester and Test Fixture Board Qualification Records**

Retain the waveform records until the next re-qualification or the duration specified by the user's internal record-keeping procedures.

### **5.7.2 Periodic Waveform Check Records**

Retain the periodic waveform records for at least one year for the duration specified by the user's internal record-keeping procedures.

## **5.8 Safety**

### **5.8.1 Initial Set-up**

**DURING THE INITIAL EQUIPMENT SET-UP, A SAFETY ENGINEER OR APPLICABLE SAFETY REPRESENTATIVE SHALL INSPECT THE EQUIPMENT IN ITS OPERATING LOCATION TO ENSURE THAT THE EQUIPMENT IS NOT OPERATED IN A COMBUSTIBLE (HAZARDOUS) ENVIRONMENT.**

### **5.8.2 Training**

**ALL PERSONNEL SHALL RECEIVE SYSTEM OPERATIONAL TRAINING AND ELECTRICAL SAFETY TRAINING PRIOR TO USING THE EQUIPMENT.**

### **5.8.3 Personnel Safety**

**THE PROCEDURES AND EQUIPMENT DESCRIBED IN THIS DOCUMENT MAY EXPOSE PERSONNEL TO HAZARDOUS ELECTRICAL CONDITIONS. USERS OF THIS DOCUMENT ARE RESPONSIBLE FOR SELECTING EQUIPMENT THAT COMPLIES WITH APPLICABLE LAWS, REGULATORY CODES, AND BOTH EXTERNAL AND INTERNAL POLICY. USERS ARE CAUTIONED THAT THIS DOCUMENT CANNOT REPLACE OR SUPERSEDE ANY REQUIREMENTS FOR PERSONNEL SAFETY.**

**GROUND FAULT CIRCUIT INTERRUPTERS (GFCI) AND OTHER SAFETY PROTECTION SHOULD BE CONSIDERED WHEREVER PERSONNEL MIGHT COME INTO CONTACT WITH ELECTRICAL SOURCES.**

**ELECTRICAL HAZARD REDUCTION PRACTICES SHOULD BE EXERCISED, AND PROPER GROUNDING INSTRUCTIONS FOR EQUIPMENT SHALL BE FOLLOWED.**

## **6.0 CLASSIFICATION PROCEDURE**

The devices used for classification testing shall have completed all normal manufacturing operations. A flow chart for this procedure is given in Annex D. Testing shall be performed using an actual device chip. It is not permissible to use a test chip representative of the actual chip or assign threshold voltages based on data compiled from a design library or via software simulations. ESD classification testing shall be considered destructive to the device, even if no device failure is detected. Devices used for HBM stressing should not have been used for any prior stress other than HBM at a lower voltage. Results obtained using parts already submitted to stress other than HBM may be affected.

NOTE: Test chip, in this case, means ESD test structure.



## 6.1 Parametric and Functional Testing

Prior to ESD stressing, parametric and functional testing using conditions required by the applicable part drawing or test specification shall be performed on all devices submitted. Parametric and functional test results shall be within the limits stated in the part drawing for these parameters.

### 6.1.1 Handling Devices

ESD damage prevention procedures shall be used before, during, and after HBM and post parametric testing.

NOTE: See the latest revision of ANSI/ESD S20.20, JESD625, or IEC61340-5-1 for guidance.

## 6.2 Device Stressing

There are two major methods for device stressing. The traditional approach is based on knowledge of device pin function and is referred to as pin combination stressing. This method and its variations are described in Section 6.3.

The second method is “pin-pair” stressing. This method is covered in Section 6.6. Pin-pair testing is required for discrete devices (FETs, transistors, etc.) and integrated circuits with 10 pins or less (including no-connects). Pin-pair stressing is allowed for devices of any pin count. No-connects shall still be excluded from testing as described in Section 6.2.1.

A sample of three devices for each voltage level shall be characterized for the device ESD withstand threshold using the voltage levels shown in Table 1. Finer voltage steps may optionally be used to obtain a more accurate measure of the withstand threshold and improve the detection of devices exhibiting failure windows (see Annex E). It is recommended that ESD testing starts at the lowest level in Table 1 for failure window detection, but testing may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 1, and the device fails at the initial voltage, testing shall be restarted with three new devices at the next lowest level. For example, if the initial voltage is 1000 volts and the device fails, restart the test at 500 volts. The ESD test shall be performed at room temperature.

NOTE: It is recommended to verify continuity between device pins and the socket after inserting devices to be tested. Leakage measurements or curve tracing may be used.

For each voltage level, a sample of three devices shall be stressed using at least one positive and at least one negative pulse. A minimum of 100 milliseconds between pulses per pin for all pin combinations specified in Table 2 or between pin pairs if using the pin-pair test method should be used. Separate samples may be used for different polarities or different pin combination sets.

NOTE: References to Table 2 in this section refer to the use of either Table 2A or Table 2B.

NOTE: In some ESD simulators, a charge removal circuit is not present. For these simulators, increasing the time between pulses to prevent a charge build-up is one method to reduce the risk for subsequent pin overstress. Alternatively, performing curve trace leakage tests after each pulse will also remove this excess charge stored in the test fixture board or socket.

Three new devices may be used at each voltage level or pin combination if desired. This will help reduce any step-stress hardening effects and reduce the possibility of early failure due to cumulative stress. In isolated cases, it is possible for failure windows to exist below the determined withstand threshold. See Informative Annex E for methods that can be used for failure window detection. It is permitted to partition further each pin combination set in Table 2 and use a separate sample of three devices for each subset within the pin combination set.

It is permitted to partition testing of devices among different testers as long as all testers are qualified (per Section 5.3) and all required stressing is performed (pin combinations of Table 2 or all pin pairs) on at least one set of three devices. It is desirable to report a withstand threshold for a subset of pins or pin combinations in some cases. A method for doing this is described in Annex B.

### 6.2.1 No-Connect Pins

Verified no-connect pins shall not be stressed and shall be left floating at all times.

Some pins labeled as no connect, such as thermal pads, are actually connected to the die. These shall be stressed. When pin combination stressing is used, these shall be classified as a supply pin or non-supply pin described in Section 6.3.

### 6.3 Pin Combination Stressing

When using the pin combination method, there are two options, Table 2A and Table 2B. Table 2A has advantages in terms of test time by reducing the total number of stresses to the device under test. The reduction in the number of stresses also reduces wear out of devices due to repetitive stressing of circuit elements shared in the current paths of multiple pin combinations. Table 2A, however, requires more detailed knowledge and understanding of the device and may not be practical in all cases. In these situations, Table 2B may be used. Table 2B is the legacy pin combination set described in ANSI/ESDA/JEDEC JS-001-2010 and earlier HBM test methods.

Furthermore, device stressing can be done using a combination of Table 2A and Table 2B. For example, one could use pin combination set 1 through N from Table 2A and set N+1 from Table 2B. Additional information and guidance on the use of the pin combinations are given in Annexes A and C. The test results, actual pin combination sets used, the tester(s) used, and all tester settings necessary to reproduce the test shall be recorded and maintained according to company recordkeeping procedures.

Setting up the pin combination test plan requires knowledge of the device under test (see Annex D). Each pin of the device shall be classified as a no connect, supply pin, or non-supply pin. These pin categories are defined in Sections 6.3.1 through 6.3.3. Additionally, supply pins shall be grouped into supply pin groups as described in Section 6.4.1. With this basic knowledge, testing may be done using Table 2B. With additional knowledge of the device to be tested, associated supplies may be defined as described in Section 6.5.1.1. With associated supplies defined, lines 1 to N of Table 2A may be used. Table 2A also eliminates non-supply to non-supply testing except for special cases discussed in Section 6.3.3.1.

#### 6.3.1 “No-Connect” Pins

Pins labeled as no connect but found to have an electrical connection to the die shall be:

- Classified as a supply pin if metallically connected to a supply pin.
- Classified as a non-supply pin if not metallically connected to a supply pin.

#### 6.3.2 Supply Pins

A supply pin is any pin that provides current or a current return path to the circuit. Many supply pins are labeled as such and can be easily recognized as supply pins. Examples include VDD, VDD1, VDD2, VDD\_PLL, VCC, VCC1, VCC2, VCC\_ANALOG, GND, AGND, DGND, VSS, VSS1, VSS2, VSS\_PLL, VSS\_ANALOG, etc. Others are not and require engineering judgment based on function in the normal circuit operation (examples include Vbias, Vref, etc.). Supply pins typically transmit no information, such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

An example of a pin that appears to be a supply pin but may be treated as a non-supply pin is the VPP pin on EPROM memories. The VPP puts the memory into a special, rarely used programming state and provides the high-voltage needed for programming the memory.

##### 6.3.2.1 Other Supply Pin Types

Any pin intended to be pumped above the positive supply or below the negative supply of its circuit block shall be treated as a supply pin (for example, positive and negative terminal pins connected to a charge pump capacitor).

Any pin connected to an internal power bus (or a power pin) by metal, as described in Section 6.3.2, shall be treated as a supply pin (for example, a Vdd sensing pin).

Any pin intended to supply power to another circuit on the same chip shall be treated as a supply pin. However, if a pin is intended to supply power to a circuit on another chip but not to any circuit on the same chip, it may be treated as a non-supply pin.

### 6.3.3 Non-Supply Pins

All pins not categorized as supply pins or no connects are non-supply pins. This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit or receive information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

#### 6.3.3.1 Direct Coupled Non-Supply Pin Pairs

A coupled non-supply pin pair may have a potential ESD current path that does not involve supply rails. These include analog and digital differential pairs and other special function pairs (for example, D+/D-, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP\_DP/CCN\_DN, etc.). Coupled non-supply pin pairs are device-specific, and not all devices will have these.

1. Any non-supply pin pairs that may have current paths in between that do not involve the supply rails. This path may be through functional devices or parasitic paths.
2. Non-supply pin pairs directly interfacing with each other, such as differential inputs or differential outputs.
3. Non-supply pin pairs that have a current path in between that consists of a single transistor or capacitor.

NOTE: Engineering judgment should be used to identify all coupled non-supply pin pairs. See ESDA/JEDEC JTR001 for a more extensive list of examples for coupled non-supply pins.

## 6.4 Pin Groupings

### 6.4.1 Supply Pin Groups

The supply pins are partitioned into supply pin groups with each supply pin defined as a member of one and only one supply pin group. A supply pin that is not connected by metal to any other pins forms a single pin supply pin group. Supply pins interconnected by metal on the chip or within the package form a supply pin group. The metal interconnects should be verified through reliable device documentation. However, excessive metal trace resistance in the die interconnect associated with grouping these pins could mask an ESD protection weakness in HBM testing.

NOTE: If the pin interconnect design is unknown, either measure the resistance between supply pins to determine the supply pin groups or treat each pin as a separate supply pin group.

NOTE: If the resistance between any two pins is greater than 3 ohms, the pins should be placed into separate supply pin groups. The resistance is measured between any two supply pins with the same name. If there are more than two pins, then the worst-case resistance should be determined by measurement.

#### 6.4.1.1 Partitioning Supply Pin Groups

Pins of a supply pin group may be divided into two or more subgroups such that each pin is a member of at least one subgroup. This partitioning may result in each pin being in its own subgroup. When a supply pin group is connected to Terminal B, all pins specified for Terminal A are stressed separately to each subgroup. When dividing a supply pin group into subgroups, all the subgroups remain part of their supply pin group and are not tested against each other.

#### 6.4.1.2 Supply Pins Connected by Package Plane

If a set of supply pins are connected by a package plane, as few as one pin (selected arbitrarily) from that set of pins may be used to represent the entire set as a supply pin group. The remaining pins in the set need not be stressed nor grounded and may be left floating during all testing.

NOTE: For example, if a supply pin group of 25 pins consists of five pins connected by metal only at the die level and 12 additional pins connected with one package plane, and another with eight pins connected with a

second package plane, the group may be represented by the five die-level connected pins and at least one pin from each package plane connected sets.

NOTE: Tester parasitics may be reduced by connecting all the pins of the group to Terminal B instead of leaving the unselected pins floating. This is not necessary if a custom board has been built which isolates the unselected pins.

#### 6.4.1.3 Supply Pins Connected by an Above Passivation Layer

If a set of supply pins are connected by an above passivation layer (APL), as few as one representative pin(s) from that set of supply pins may be used to represent the entire set as the supply pin group. The remaining unselected pins in the set need not be stressed nor grounded and may be left floating during all testing as long as the APL connects all such unconnected pins with a resistance of 1 ohm or less to any other pin in the set.

#### 6.4.2 Shorted Non-Supply Pin Groups

Shorted non-supply pins connected by metal in a package plane, an APL with a resistance less than 1 ohm, and/or a common bond pad, form a non-supply pin group. One pin of this non-supply pin group (selected arbitrarily) may be used to represent the entire set of shorted non-supply pins. The remaining pins in the set need not be stressed nor grounded and may be left floating during all testing.

NOTE: This configuration is uncommon as non-supply pins typically are isolated from other pins in the package.

### 6.5 Pin Stress Combinations

When using the pin combination method, the set of pin combinations given in Tables 2A or 2B may be used.

NOTE: See ESDA/JEDEC JTR001 for more information on this topic.

Table 2A. Required Pin Combinations Sets

Pin Combination Set Number [a]	Pin(s) Connected to Terminal B (Ground)	Pin Connected to Terminal A (Single Pins, tested one at a time)
1	Supply Pin Group 1 [b, c]	Every Supply Pin except pins of Supply Pin Group 1 [c, d]  Every Non-Supply Pin Associated with Supply Pin Group 1
2	Supply Pin Group 2 [b, c]	Every Supply Pin except pins of Supply Pin Group 2 [c, d]  Every Non-Supply Pin Associated with Supply Pin Group 2
...	...	...
N	Supply Pin Group N [b, c]	Every Supply Pin except pins of Supply Pin Group N [c, d]  Every Non-Supply Pin Associated with Supply Pin Group N
N+1	One Pin of Each Coupled Non-Supply Pin Pair, one pair at a time	The other pin of the Coupled Non-Supply Pin Pair

[a] In all combinations, pins not connected to either Terminal A or Terminal B shall be left floating during the stress pulse. All no-connect pins are left floating at all times.

[b] Supply pins may be all connected together as a single group or divided into subgroups. Subgroups can be individual pins. Every Terminal A pin is stressed to each of these subgroups (see Section 6.4.1).

[c] A single pin may be used from supply pin groups known to be interconnected by a package plane or APL (see Sections 6.4.1.2 and 6.4.1.3).

[d] Supply pin-to-supply pin combinations may be stressed using only single polarity pulses (see Section 6.5.1.2).

Table 2B. Legacy Pin Combinations Sets

Pin Combination Set Number [cc]	Pin(s) Connected to Terminal B (Ground)	Pin Connected to Terminal A (Single Pins, tested one at a time)
1	Supply Pin Group 1 [aa]	Every Supply Pin except pins of Supply Pin Group 1 [aa]  Every Non-Supply Pin
2	Supply Pin Group 2 [aa]	Every Supply Pin except pins of Supply Pin Group 2 [aa]  Every Non-Supply Pin
...	...	...
N	Supply Pin Group N [aa]	Every Supply Pin except pins of Supply Pin Group N [aa]  Every Non-Supply Pin
N+1	All Non-supply Pins, except PUT [bb]	Each Non-Supply Pin (as the PUT)

[aa] A single pin may be used from supply pin groups known to be interconnected by a package plane or APL (see Sections 6.4.1.2 and 6.4.1.3).

[bb] Non-supply pins connected to Terminal B can be divided into subsets, such that each of these pins is a member of at least one subset. Every Terminal A pin is stressed to each of these subsets.

[cc] All pins not connected to either Terminal A or Terminal B shall be left unconnected (floating pins) during the stress pulse. All no-connect pins are unconnected at all times.

#### 6.5.1 Non-Supply and Supply to Supply Combinations (1, 2...N)

Tables 2A and 2B are organized by the DUT's N supply pin groups. The first N rows of these tables have one unique supply pin group tied to Terminal B. When pins are not connected by a package plane, pins within a supply pin group shall be stressed individually (when connected to Terminal A). When tied to Terminal B, as shown in tables, these pins shall be connected either individually, or in groups, or tied together at the test board level.

##### 6.5.1.1 Association of Non-Supply Pins with Supply Pin Groups (Table 2A only)

Each non-supply pin is associated with one or more supply pin groups (Section 6.4.1). For example, for an I/O pin, the output drivers of the pin connect to the VCCIO supply group while the input receiver of the same pin connects to the VCC supply group. Additionally, this I/O pin may be connected to one or more grounds (for example, VSS, VSSIO). The design team typically provides this information.

A non-supply pin is associated with a supply pin group if either:

- a. The connection to that supply pin group is necessary for the function of the circuit.
- b. A parasitic path exists between the non-supply and supply pin group (for example, open-drain type non-supply pin to a VCC supply pin group that connects to a nearby N-well guard ring).

In the testing described in Table 2A, non-supply pins are only stressed against the supply pin groups with which these are associated. If the information on the association with supply pin groups for each non-supply pin is known, then non-supply pins may be stressed only to their associated supply pin groups. Stressing to supply pin groups not associated with a non-supply pin is not required. If this information is not available, then every non-supply pin shall be tested to each supply pin group specified in lines 1 to N of Table 2B.

NOTE: The use of Table 2A is highly recommended for devices exceeding eight supply pin groups.

NOTE: Pin combinations 1 to N in Table 2B treats all non-supply pins as being associated with every supply pin group.

NOTE: See ESDA/JEDEC JTR001 for practical examples.

#### 6.5.1.2 Stress Polarities of Supply Pins (Tables 2A and 2B)

When pins of supply pin groups are stressed to other supply pin groups, it is permissible to perform all stresses with a single polarity.

NOTE: For some devices under test it has been found that power supply stress with one polarity is more susceptible to tester parasitics than the opposite polarity. These parasitic currents can cause waveform distortion and anomalous test results. Since every supply is stressed on Terminal A with respect to every other supply on Terminal B, all supply pairs are normally tested twice. For low resistance power supply busses the positive stress of power Group 1 on Terminal A versus power supply Group 2 on Terminal B is essentially redundant to negative stress of power supply Group 2 on Terminal A versus power supply Group 1 on Terminal B. Removing this testing redundancy allows testing only with the polarity which minimizes tester parasitic. For most technologies, such as CMOS circuits on p substrates, positive only testing is preferred. For some technologies, negative only testing may be preferred. Refer to ESDA/JEDEC JTR001 for further information.

#### 6.5.1.3 Alternative Pin Stress Method for Non-Supply Pins (Tables 2A and 2B)

A non-supply to supply pin stress may be replaced by its corresponding supply pin to non-supply pin stress. If only a single polarity stress is being replaced, the opposite polarity stress shall be used. As non-supply pins are not typically tied to other pins, this will require each supply pin of the supply pin group to be stressed to each non-supply pin individually. If the non-supply pin is tied to other pins, as noted in Section 6.4.2, all other non-supply pins of the group shall be left floating.

NOTE: Typically, the non-supply to supply pin negative polarity stress will be replaced with the supply to non-supply pin, positive polarity stress. This allowance is useful when tester parasitic capacitances impact the slew rate of the HBM pulse.

NOTE: If this alternative test method is used on a supply pin group with more than a small number of pins, tester parasitic capacitance will increase (that is, slow down) the rise time of the signal. Longer rise times may cause dynamic ESD protection circuits not to function properly (see Annex C.4).

#### 6.5.1.4 Cloned Non-Supply (Cloned IO) Pin Reduction Sampling Method

Some non-supply pins may be removed from HBM testing if the criteria of cloned IO are met, as explained in Annex A. The user shall identify the required sampling pins. 30 randomly selected non-supply pins shall be tested for each set of cloned IOs (M). HBM stresses will be applied to the selected pins according to Table 2A or 2B. The remaining M-30 pins are not stressed and remain floating at all times. The detailed steps are in Annex A.



### **6.5.2 Non-Supply to Non-Supply Combination**

Pin combination set N+1 in Table 2A specifies to stress each coupled non-supply pin pair.

#### **6.5.2.1 Alternative Non-Supply to Non-Supply Combinations**

If the information on non-supply pins to determine coupled pairs is not available, the pin combination set N+1 in Table 2B shall be used. This specifies to stress each non-supply pin individually (Terminal A) with all other remaining non-supply pins tied together and connected to Terminal B, except for those shorted non-supply pins that are metalically connected to the pin under stress on the die, which will be left open as specified in Section 6.4.2.

##### **6.5.2.1.1 Shorted Non-Supply Pins (Table 2B only)**

If using Table 2B for a device with shorted non-supply pins connected on the die only and bonded out to multiple separate pins, these pins shall be stressed individually according to combination set N+1 with the remainder of these connected pins left floating. If using Table 2B for a device with shorted non-supply pins connected by a package plane, APL with resistance less than 1 ohm, or share a common bond pad, one of these pins (selected arbitrarily) may be used to represent the entire set of shorted non-supply pins. The remaining pins in the set need not be stressed nor grounded and should be left floating during all testing.

##### **6.5.2.1.2 Partition Allowance for Non-Supply Pins (Table 2B only)**

When using Table 2B, it is permitted to partition the non-supply pins to be connected to Terminal B into two or more subsets, such that each of these pins is a member of at least one subset. The subsets may be single pins. The pin connected to Terminal A is to be stressed to each of these subsets separately. This process is repeated for each non-supply pin.

### **6.6 Pin-Pair Stressing**

All pin pairs shall be stressed for all devices under stress using at least one positive and one negative pulse with a minimum of 100 milliseconds between pulses. The pin pair's first pin shall be connected to Terminal A of the tester's pulse generator circuit and the pin pair's second pin shall be connected to Terminal B (ground). True no-connects are not to be stressed.

NOTE: Table 2A and Table 2B are only valid for ICs having more than 10 pins.

### **6.7 Low-Parasitic HBM Simulator Allowance**

If a simulator meets the requirements in Section 4.2.1 for an N-channel low-parasitic HBM simulator, then when stressing a pin pair, selecting which pin is on Terminal A and which is on Terminal B is not significant. After stressing a pin pair using a low parasitic HBM simulator, using both polarities, it is permissible to omit the reverse stress of the pins. For example, if pin X is stressed on Terminal A to pin Y on Terminal B with both voltage polarities, it is unnecessary to stress pin Y on Terminal A with pin X on Terminal B. This also applies to pin pairs resulting from using Table 2A or 2B.

### **6.8 Testing After Stressing**

If a different sample group is tested at each stress level, it is permitted to perform the DC parametric, and functional testing after all sample groups have been ESD tested.

## **7.0 FAILURE CRITERIA**

A part is defined as a failure if it fails the datasheet parameters using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.



## 8.0 DEVICE CLASSIFICATION

According to the HBM withstand voltage, ESD sensitive devices are classified regardless of polarity, as defined in Table 3. A device can be classified based on testing with any HBM simulator that meets all the parameters of Section 4.0. If a device tests to a higher classification level on one HBM simulator than another, it is assigned the higher classification.

NOTE: If different classification levels are seen from multiple testers, it is recommended to investigate further.

**Table 3. HBM ESD Device Classification Levels**

Classification	Voltage Range (V)
0Z	< 50
0A	50 to < 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

## ANNEX A (NORMATIVE) – CLONED NON-SUPPLY (IO) PIN SAMPLING TEST METHOD

This test method is targeted for IC designs with a uniform approach to ESD protection where the same IO cell design is replicated in a set of pins. This approach works well for high pin count devices with wide data busses such as large microprocessors. For simplicity, these types of non-supply (IO) pins with a common design are called cloned IOs. A flow chart of the method is given in Figure 6.

A statistical Excel program has been developed to simplify the statistical calculation used in this new test procedure. After the user has validated that the identical IO pins meet the definition of cloned IO pins, the user can download the Excel file from the Standard resources section at <https://www.esda.org/standards/>. Read ESDA/JEDEC JTR001 to learn how to use the statistical Excel file.

### A.1 Pin Sampling Overview and Statistical Details

The ESD sensitivity level of cloned IOs can be determined to a high degree of confidence (99%) by HBM stressing a statistically significant pins sample compared to stressing 100% of these identical pins. This test method divides the total number of cloned IO pins into single or multiple sets. The total number of pins within a single set is defined as M.

The sampling test method starts by selecting 30 pins (n) at random from all cloned IO pins. HBM tests are performed on the selected pins where a failure is defined as significant increases in pin leakages or changes in the curve trace curves. One IC device is used to determine the failure distribution of the group of cloned IOs. The average failure voltage, mean, and the range (the failure voltage difference between the weakest and the strongest pins) of this sample are found from the measured failure voltages. The HBM stress voltages are incrementally increased by steps of ~100 volts until at least 15 pins out of the sample of 30 pins have failed.

Now there is enough data to apply statistics to determine the likelihood that all M cloned pins, including all the untested (M-30) pins will pass a target specification limit (SPL). If the probability of all cloned pins passing the target stress level is 99% or greater, then the sample size of 30 randomly selected cloned IO pins can be used for all subsequent HBM testing. If the probability is not at least 99%, or if the weakest pin tested doesn't pass at least 50% higher than the target HBM voltage level, this procedure shall not be used.

The statistics applied in this method are based on the assumption that failure voltages among a set of cloned IO pins are independent and normally distributed. The mean and range of the sampled pins provide a good estimate for the mean and standard deviation of the entire set of cloned IO pins.

The mean of the sample is known when at least half of the sampled pins have failed, and this fail voltage (VM) can be used to represent the mean of the total cloned pin population with a high confidence level (99%). The failure voltage difference from the lowest failure voltage (V1) to where at least half of the sampled pins fail (VM) is half the range. The range is defined as V2-V1, where V2 is the highest failure voltage where all 30 pins would fail, and  $V2-V1=2[VM-V1]$ .

The standard deviation, Sigma, of the cloned IO pin population is found from the relationship between the range of a sample and the sample size. The statistical function, d2, provides the expected ratio of the range of a sample to the standard deviation of the population. With a sample size of n=30, d2 is 4.086; therefore, the calculated standard deviation (sigma) is  $[VM-V1]/2.043$ .

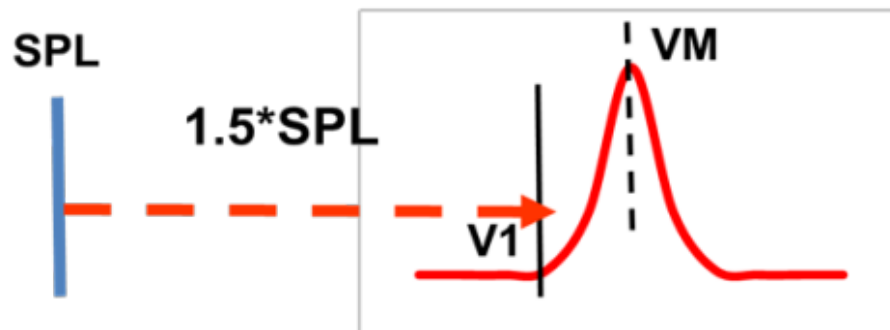
The probability of untested pins passing a target level (SPL) with a high confidence level (99%) is found in the Standard Normal Cumulative Distribution Function. The steps necessary to do this calculation are as follows:

1. Calculate the number of standard deviations (z) between the Mean and SPL voltage levels:  

$$z = [VM-SPL]/\text{sigma (see Figure 5)}$$
2. Use either a normal cumulative distribution table or an Excel spreadsheet and the Excel NORMSDIST function to calculate the probability that any single pin in the population will not pass SPL. This is defined as NORMSDIST (-z). This value is the area of the normal distribution where the failure voltages are less than SPL.

3. The probability that any single pin selected at random will pass the SPL is  $[1 - \text{NORMSDIST}(-z)] = \text{NORMSDIST}(z)$ .
4. Since we have  $M-n$  untested pins, the probability that all untested pins will pass SPL is  $[\text{NORMSDIST}(z)]^{(M-n)}$ .
5. If  $[\text{NORMSDIST}(z)]^{(M-n)} \geq 0.99$ , then the sample data shows that all cloned IO pins for this IC device will pass the HBM voltage SPL with 99% statistical confidence.

If these calculations show that the 99% confidence level can be met, this sampling HBM test procedure for cloned IO pins can be applied. Subsequent HBM testing using three parts can follow the standard HBM test procedures, but only a random selection of 30 pins of the cloned IO pin set needs to be stressed, and the remaining cloned IOs may be left “floating” during all HBM tests.



*Figure 5: SPL, V1, VM, and z with the Bell Shape Distribution Pin Failure Curve*

## A.2 IC Product Selections

An IC product is a possible candidate to apply this test method if the identical IO pins can be shown to meet the definition of Cloned IO defined in Section 3.0. Consult with the IC design team and/or ESD team to confirm that the set of IO pins meets the definition. Once confirmed, determine how many cloned IO pins are in the set, called  $M$ . Use the sampling test method only if  $M \geq 50$  pins.

Ensure that none of these IO clones have a feedthrough connection to internal transistors, and if so, then those pins have to be excluded from the test group. Design verification can be done manually, but a more efficient check can be done through software checkers that identify cloned IO pins with an associated macro name.

Pad cell designs may be designed with feedthrough metal lines. These lines allow internal devices not in the pad cell to be metallurgically connected to the bond pad. As these additional devices may create ESD current paths unique to each pin, pins using these pad cells shall not be considered IO clones.

## A.3 Randomly Select and Test Cloned IO Pins

Select 30 cloned IO pins at random from the total population of  $M$  pins. A spreadsheet-based random number generator may be used. Do not attempt to use any other selection criterion such as purposeful selection of IOs close to or farther from VSS/VDD pads.

Determine the HBM voltage target spec level for this product (SPL) from the datasheet or other documentation. A shift in IV curves may be used as the basis for failure detection to determine a  $V1$  and  $VM$  (mean) point if it is cost-prohibitive in terms of test time to verify the full datasheet parameters.

One IC device will be HBM stressed to determine the minimum HBM fail voltage ( $V1$ ) and mean HBM fail voltage, where 15 out of 30 of the sample IO pins fail. Write an HBM test program that will test all sample cloned IO pins to their associated supply pins. Start HBM stressing at  $1.5 \times \text{SPL}$  and

stress all selected pins positively and negatively. After stressing each pin, measure the DC leakage values or curve trace curves and determine if the HBM failure criteria have been met.

If any pin fails at  $1.5 \times \text{SPL}$ , do not use the sampling test procedure. Increase the HBM voltage stress in steps of 100 volts or 10% of SPL, whichever is greater. Keep stressing all selected pins at the increasing stress levels to find the maximum voltage level where no pins fail – call this V1. Continue to HBM stress all selected pins that have not failed at increasing levels to find the minimum voltage step where 15 or more pins fail – call this VM.

#### **A.4 Determine if Sampling can be Used**

**A.4.1** Using the supplied Excel spreadsheet - Use the Excel spreadsheet to determine the probability that all untested cloned IOs will pass SPL. Input M, SPL, V1, and VM into the program to obtain the confidence level. If the confidence level is 99% or greater, the cloned sampling HBM test method can be used. If not, then do not use this test method.

**A.4.2** Without using the Excel spreadsheet - Using the values of: M, SPL, V1, VM,  $n=30$ , and  $d2=4.086$  derived from the stressing of 30 pins determine if the confidence level is 99% or greater using the following steps:

1. Derive the estimated range;  $\text{Range}=2 \times (\text{VM}-\text{V1})$ .
2. Derive the estimated sigma;  $\text{sigma} = \text{Range}/4.086$ .
3. Determine the number of sigmas the mean VM is above the SPL,  $z = (\text{VM}-\text{SPL})/\text{sigma}$ .
4. From a Standard Normal Cumulative Distribution Function Table determine the probability that all of the untested pins are above SPL by taking the single pin normal distribution probability value to the power of  $(M-30)$ , namely  $(\text{NORMSDIST}(z))$  raised to the power  $(M-30)$ . If this value is greater or equal to 0.99, then the sampling method can be used in subsequent HBM testing. If not, then do not use this test method.

#### **A.5 HBM Testing with a Sample of Cloned IO Pins**

If the set of cloned IO pins has been tested per A.3 and has been shown to meet the requirements for the sampling test method as described in A.4, then randomly select 30 cloned IO pins from the set of M cloned IO pins for full HBM testing.

The unselected  $M-30$  pins are removed from the HBM test pin list (can be listed as no-connect pins). If unwanted IC–tester interactions are known, special test fixture boards can be built that do not wire the “floating” cloned IO pins to the signal pins of the HBM test simulator. This special test fixture board will truly float the non-stressed cloned IO pins. Perform a full HBM test with all combinations using the 30 randomly selected cloned IO pins described in Section 6.3.

NOTE: The statistical Excel file can be downloaded from the Standards Resources web page on EOS/ESD Association, Inc. website, [www.esda.org](http://www.esda.org).

#### **A.6 Examples of Testing with Sampled Cloned IOs**

##### **Example 1**

A product with a large number of cloned IO pins is analyzed for possible cloned IO pin sampling. The product has 292 cloned IO pins. HBM step stress testing of 30 randomly selected cloned IO pins on one part to 50% failures found the critical parameters:  $V1=2100$  volts,  $VM=3100$  volts, with  $\text{SPL}=1000$  volts. These values are entered into the Excel spreadsheet, and the confidence level was determined to be  $> 99\%$  (99.7665%). This indicates that 30 pins may be randomly chosen to represent the 292-set of cloned IO pins.

Test 30 clone pins until 15 fail	n	30
Total count of clone pins	M	292
Lower Spec Limit in volts	SPL	1000
Highest voltage at which all 30 pins pass	V1	2100
Lowest voltage at which at least 15 pins fail	VM	3100
Estimated range		2000
d2		4.086
Estimated sigma		489.4762604
Estimated mean		3100
How many sigmas from SPL to mean?	Z	4.2903
Probability that one untested pin is above the SPL?	Prob(1)	0.999991078
Count of untested pins	(M-n)	262
Probability that all untested pins are above the SPL?	Prob(M-n)	0.997665261
If this value is > 0.99, we feel 99% confident that all the untested pins are above the SPL.		YES

Without the Excel spreadsheet, the Range is calculated from  $2 \times (VM - V1)$ , or Range = 2000 volts. The sigma is calculated from  $2000 / 4.086$  ( $n=30$ );  $\sigma=489.4762$  volts. The number of sigma between the mean and SPL is  $z = (VM - SPL) / \sigma$ , or  $z = (3100 - 1000) / 489.4762 = 4.2903$ . The probability of all untested pins being above SPL is  $NORMSDIST(4.2903)^{(292-30)} = 0.997665$ . Since the confidence level exceeds 99%, 30 pins may represent the 292-set of cloned IO pins.

### Example 2

A product with 300 cloned IO pins is analyzed for possible cloned IO pin sampling. The HBM testing of cloned IOs to failure on one part found the critical parameters:  $V1 = 1800$  volts,  $VM = 3000$  volts, with an  $SPL = 1000$  volts. These values are entered into the Excel spreadsheet, and the confidence level was determined to be < 99% (91.4538%). Therefore, this set of cloned IOs does not qualify for sampling, and the standard HBM procedure without sampling shall be followed.

Test 30 clone pins until 15 fail	n	30
Total count of clone pins	M	300
Lower Spec Limit in volts	SPL	1000
Highest voltage at which all 30 pins pass	V1	1800
Lowest voltage at which at least 15 pins fail	VM	3000
Estimated range		2400
d2		4.086
Estimated sigma		587.3715125
Estimated mean		3000
How many sigmas from SPL to mean?	Z	3.405
Probability that one untested pin is above the SPL?	Prob(1)	0.99966918
Count of untested pins	(M-n)	270
Probability that all untested pins are above the SPL?	Prob(M-n)	0.914538008
If this value is >0.99 we feel 99% confident that all the untested pins are above the SPL.		<b>NO</b>

Without the Excel spreadsheet, the Range is calculated from  $2 \times (VM - V1)$ , or Range = 2400 volts. The sigma is calculated from  $2400/4.086$  ( $n=30$ );  $\sigma=587.37$  V. The number of sigma between the mean and SPL is  $z = (VM - SPL)/\sigma$ , or  $z = (3000 - 1000)/587.37 = 3.405$ . The probability of all untested pins being above SPL is  $NORMSDIST(3.405)^{(300-30)} = 0.9145$ . Since 91.45% is less than 99%, this set of cloned IOs does not qualify for sampling, and the standard HBM procedure without sampling shall be followed.

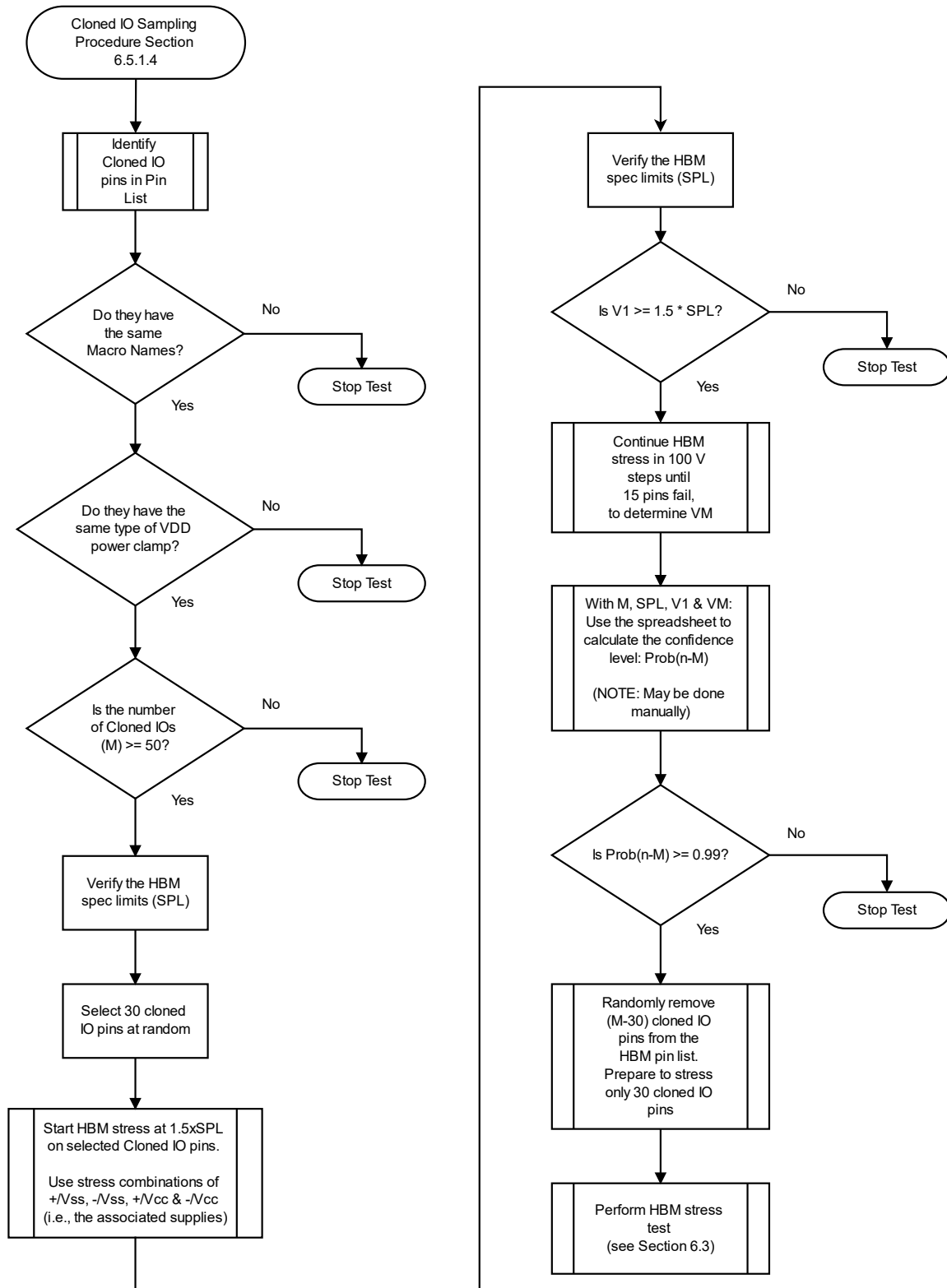


Figure 6: IO Sampling Test Method Flow Chart

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**ANNEX B (NORMATIVE) - DETERMINATION OF WITHSTAND THRESHOLDS FOR PIN OR PIN-COMBINATION SUBSETS****B.1 Introduction**

ANSI/ESD SP5.0, “For Electrostatic Discharge Sensitivity Testing: Reporting ESD Withstand Levels on Datasheets”, gives recommendations on how to report separate ESD withstand levels for special subsets of pins or pin combinations. This Normative Annex provides instructions for performing HBM testing on devices to enable this segmented threshold reporting. This procedure intends to accommodate the identification of lower passing levels for signal pins, which, due to functional requirements, cannot be designed with the same withstand levels as other pins on the device.

This method requires prior knowledge of the device’s expected pin-specific ESD performance levels, such as from design information, from previous testing using all pin combinations, or testing on other devices or test structures.

In the following procedure and requirement sections Levels A, B, C, etc. may be either HBM test voltages or classification levels.

NOTE: Even when these subsets are determined, the overall device level threshold is still reported based on the lowest threshold pin or pin combination.

**B.2 Testing Procedure**

1. At Level A, the lowest withstand level to be reported:
  - Stress all pin combinations on three devices as required in Section 6.5 using either Table 2A or 2B or all pins using pin-pair testing.
  - Verify full functionality using ATE test.
  - Any pins or pin combinations passing this level may be reported as Level A.
2. At Level B, the next higher withstand level to be reported:
  - Stress all pin combinations on three devices as required in Section 6.5 using either Table 2A or 2B or all pins using pin-pair testing, excluding those that passed Level A but expected to fail Level B (from prior knowledge of part testing/design information).
  - Either new devices or the devices used in Level A testing may be used.
  - Verify full functionality using ATE test.
  - Any pins or pin combinations passing this level, except those excluded from stressing at Level B, may be listed as Level B.
3. At Level C, the next higher withstand level to be reported:
  - Stress all pin combinations on three devices as required in Section 6.5 using either Table 2A or 2B, or all pins using pin-pair testing passing this level, excluding those reported as Level A and Level B but expected to fail level C (from prior knowledge of part testing/design information).
  - Either new devices or the devices used in Level B testing may be used.
  - Verify full functionality using ATE test.
  - Any pins or pin combinations except those excluded from stressing at Level C may be listed as Level C.
4. The procedure may be repeated at additional levels, but it is expected that only two or maybe three Levels would be practical.
5. If separate sets of three devices are to be used for the different stress levels, it is permissible to perform the stressing in parallel, followed by ATE testing, if the expected withstand levels are known before testing.



### B.3 Restrictions

To declare a subset of pins as a passing at a certain threshold level, all samples stressed at that level are required to pass. No threshold level can be determined from a set of samples that has failures (that is, individual pin thresholds cannot be extracted at a stress level that had failures; even if the pins in question did not appear to fail).

### B.4 Example of Using Subset Withstand Threshold Data

This is an example of the use of pin subset threshold data as it appears in ANSI/ESD SP5.0. The example also includes charged device model (CDM) pin subset thresholds that may be reported similarly.

A 20-pin device has been evaluated using ANSI/ESDA/JEDEC JS-002 and ANSI/ESDA/JEDEC JS-001. 18 of the 20 pins pass CDM at 500 volts while two high-speed pins (here designated as pins 3 and 4) only pass 250 volts. Similarly, 18 of the pins pass HBM at 1000 volts while the same high-speed pins (3 and 4) only pass 500 volts. Table 4 describes one way of conveying these results on a datasheet.

**Table 4. Inclusion of Lower ESD Level High-Speed Pin Data**

**ESD Information for Handling of ESDS in an ESD Protected Area (Required)**

**CDM (ANSI/ESDA/JEDEC JS-002-2022):** CDM Withstand Threshold 250 volts; CDM Class C1

NOTE: The CDM withstand threshold is determined by two high-speed pins (3 and 4), which pass 250 volts. All other pins pass 500 volts.

**HBM (ANSI/ESDA/JEDEC JS-001-2023):** HBM Withstand Threshold 500 volts; HBM Class 1B

NOTE: The HBM withstand threshold is determined by two high-speed pins (3 and 4), which pass 500 volts. All other pins pass 1000 volts.

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2023)

## ANNEX C (INFORMATIVE) – HBM TEST EQUIPMENT PARASITIC PROPERTIES

### C.1 Optional Trailing Pulse Detection Equipment/Apparatus

The maximum trailing current pulse level is defined as the maximum peak current level observed through a 10-kilohm test load (current = voltage across test load divided by 10 kilohms) after the normal HBM pulse(s). After-pulse leakage, the period to be evaluated is from 0.1 to 1 millisecond after the decay of the HBM current pulse. If a spurious current pulse is observed, begin the 0.1-millisecond measurement point from the start of the spurious current pulse.

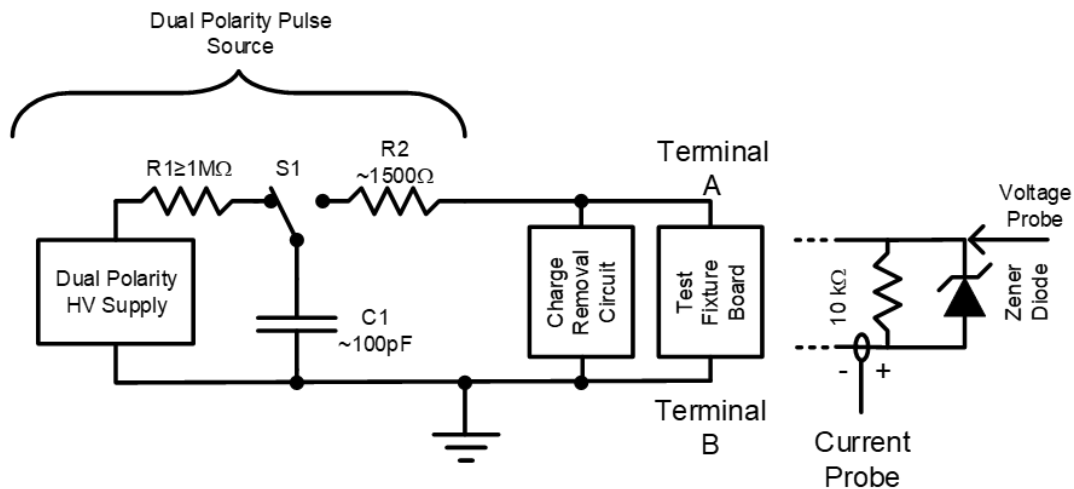


Figure 7: Diagram of Trailing Pulse Measurement Setup

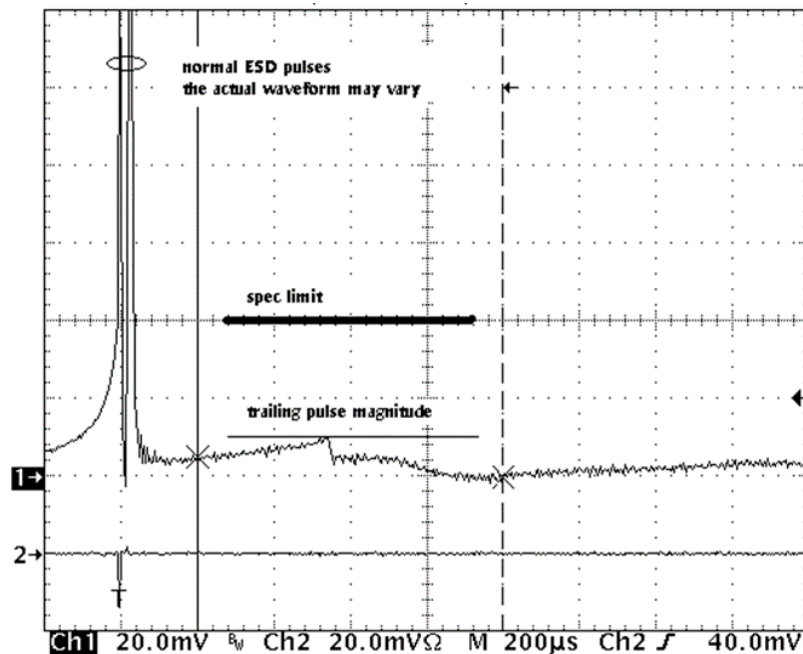
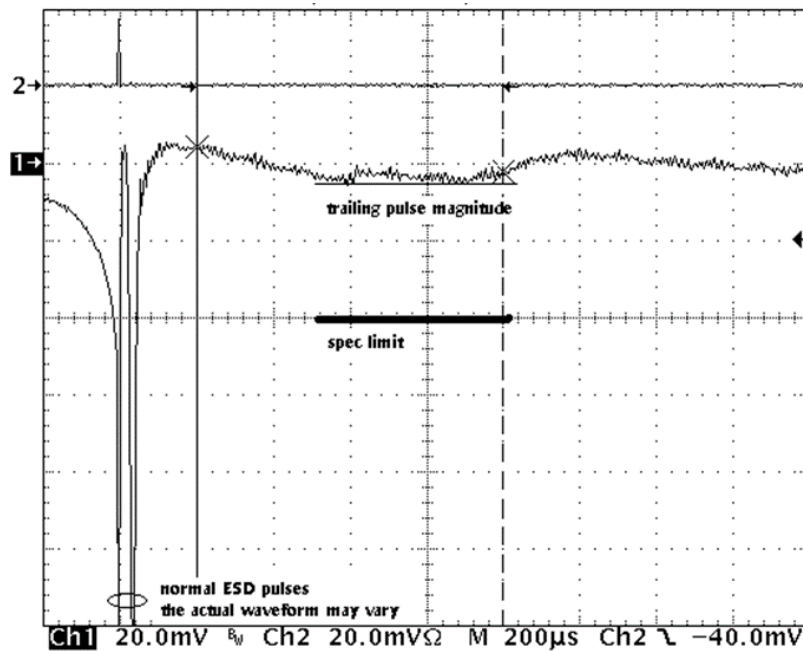


Figure 8: Positive Stress at 4000 Volts



*Figure 9: Negative Stress at 4000 Volts*

The magnitude of the trailing current pulse shall be less than four microamperes when the applied HBM stress voltage is at 4000 volts. This includes both positive and negative polarities (see Figures 8 and 9 for sample waveforms).

A circuit for measuring the trailing current pulse is shown in Figure 7. The voltage probe shall have an input impedance no less than 10 megohms, an input capacitance no larger than 10 picofarads, a bandwidth better than 1 megahertz, and a voltage rating to withstand at least 100 volts. The evaluation load resistance is 10 kilohm in value with a tolerance of  $\pm 1\%$  and can withstand up to 4000 volts. The Zener diode has a breakdown voltage range from 6 to 15 volts and a power rating from  $\frac{1}{4}$  to 1 watt.

## C.2 Optional Pre-Pulse Voltage Rise Detection Test Equipment

HBM events may exhibit a phenomenon that generates a voltage rise at the stressed pin prior to the main HBM current pulse if the pin impedance is high. In some ESD simulators, this phenomenon is unrealistically severe and may lead to inconsistent ESD threshold results. The characteristics of this pre-current pulse voltage event depend on the conditions and the environment of the arcing associated with the HBM discharge, the parasitic capacitances of the tester, and the pin impedance of the device under test. The following test equipment and apparatus are required to determine the magnitude of the resulting voltage rise (see Figure 10 for measurement setup).

The worst-case condition will be measured for a low capacitance Zener diode with a voltage in the 8- to 10-volt range. The Zener diode will protect the voltage probe, and its low capacitance does reduce the voltage buildup appreciably. The current probe on the groundside of the diode is used to trigger an oscilloscope. The voltage probe, connected to a second channel of the oscilloscope, should have high resistance such as a 10 megohm 10X probe.

Sample data is shown in Figure 11 for a 9.4-volt Zener diode. The HBM current pulse occurs at time zero and cannot be seen at this time scale. At the time scale of an HBM event, tens to hundreds of nanoseconds, the voltage before the HBM current pulse would appear as a DC voltage across the diode. To measure the voltage across a device, the Zener diode would be replaced by the device of interest.

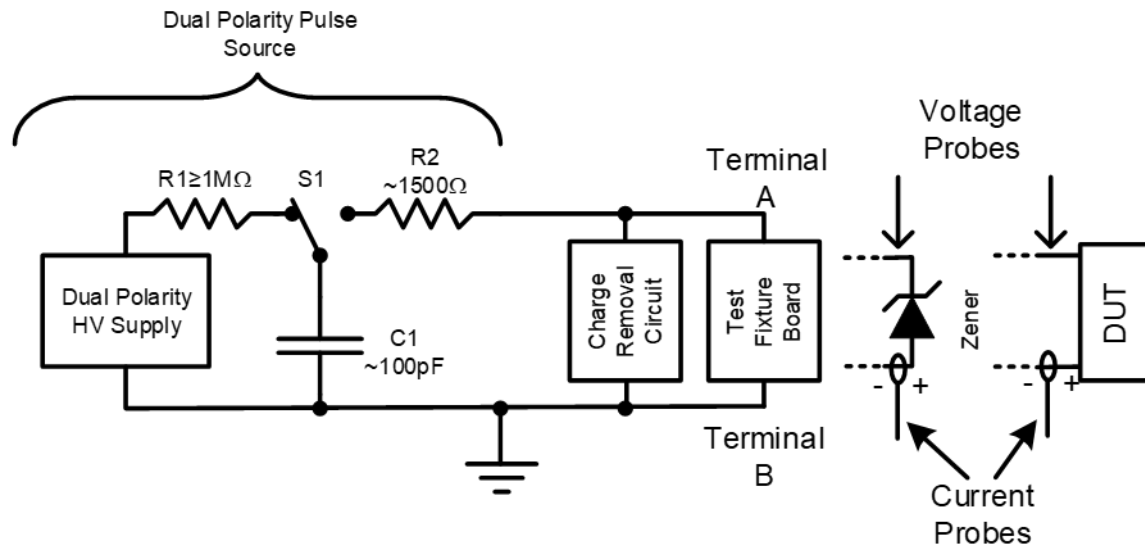


Figure 10: Illustrates Measuring Voltage before HBM Pulse with a Zener Diode or a Device

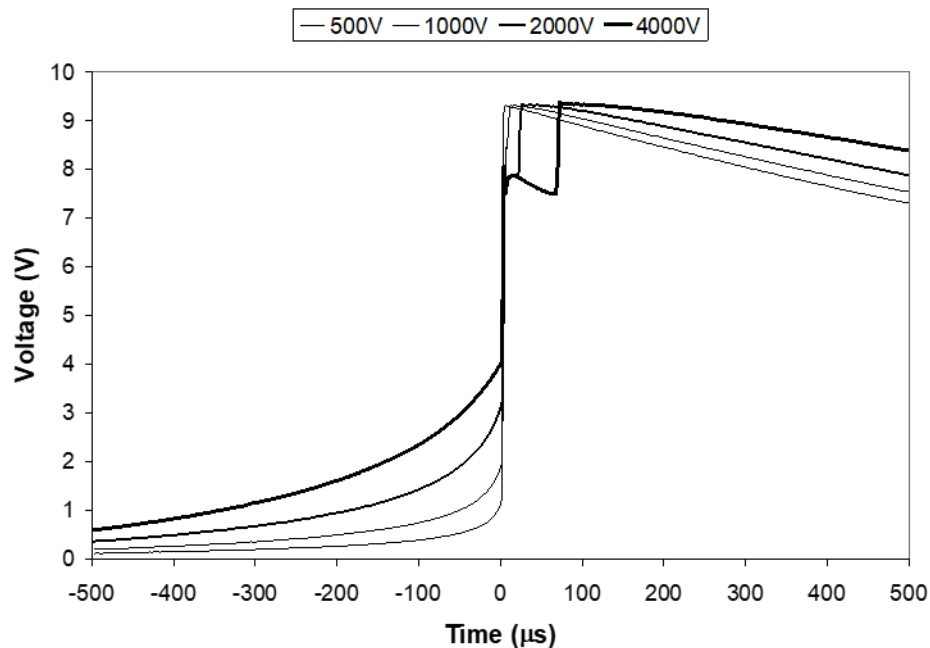


Figure 11: Example of Voltage Rise before the HBM Current Pulse across a 9.4-volt Zener Diode

### C.3 Optional Pre-HBM Current Spike Detection Equipment

Some HBM simulators may generate a pre-current pulse prior to the actual HBM current pulse at levels below 2 kilovolts. These pre-pulses may lead to inconsistent ESD threshold results. The pre-pulse is a small HBM shaped pulse however it has a much lower peak current than the actual event.

NOTE: Maximum allowed pre-pulse depends on device robustness.

This optional measurement ensures that the system being used does not demonstrate a pre-current pulse.

Using the shorting load configuration shown in Figure 12, initiate a 1000-volt pulse and verify that there is no discernible pre-current pulse. The period to be evaluated for a pre-pulse is 50 microseconds prior to the actual HBM current pulse. It is recommended to use different time base settings, first at 10 microseconds and then on a 100-nanoseconds scale to ensure no pre-pulse occurs. Note, as the pre-pulse current level is much lower than the actual HBM event, it is recommended to capture the actual HBM event, then lower the volts/div scale so that a lower amplitude pulse could be seen.

Figure 13 shows examples of pre-current pulses which occurred at different times prior to the actual HBM event.

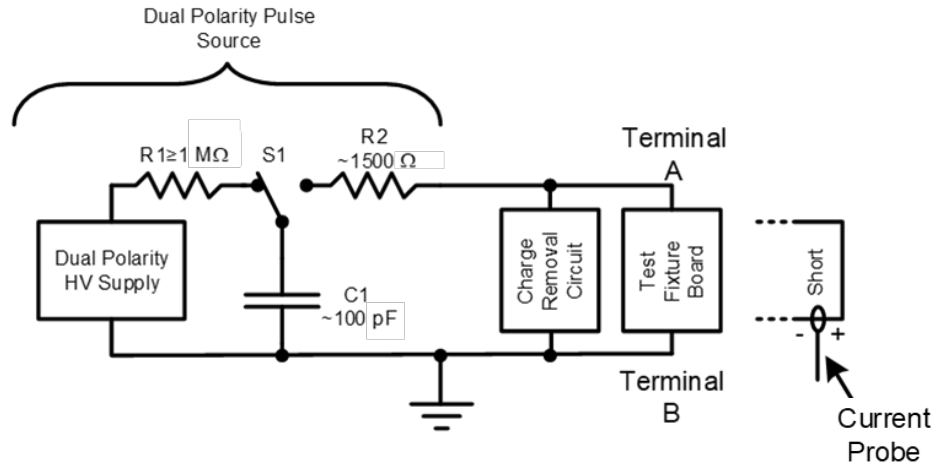


Figure 12: Optional Pre-Current Pulse Detection Equipment/Apparatus

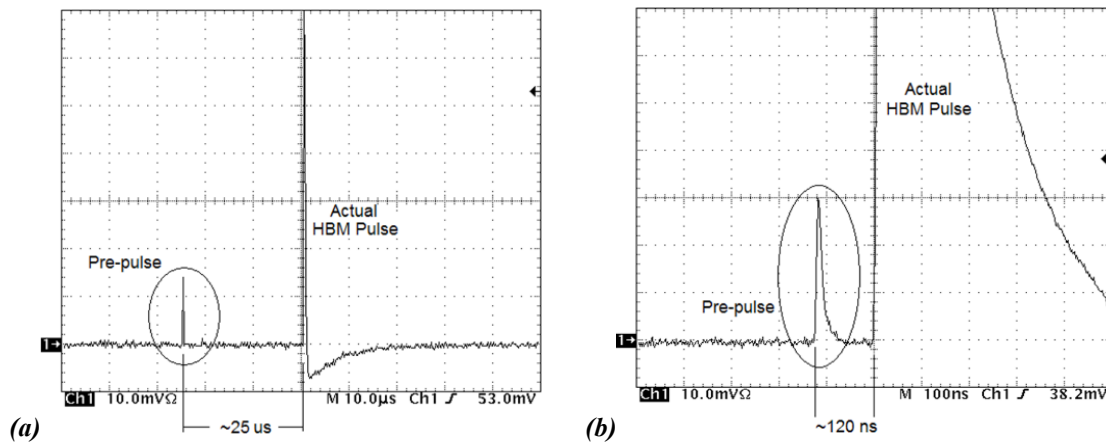


Figure 13: Positive Stress at 1000 Volts

NOTE: (a) Pre-pulse occurring 25  $\mu$ s prior and (b) Pre-pulse occurring ~120 ns prior to the actual HBM event to the actual ESD event.

#### C.4 Open-Relay Tester Capacitance Parasitics

The HBM stressing of a single supply pin is complicated when the pin is part of a group of multiple like-name supply pins (balls) shorted together via the DUT (for example, via a package plane). When the device is placed in the socket only one pin can be connected to Terminal A. The other

supply pins are left “floating” as the HBM simulator’s connect relays are opened so the other supply pins do not connect to Terminal A or B.

Recent HBM tester research on package-plane-shortened pins has found that when a single pin is stressed, the other “floating” supply pins act like small capacitors to ground. Since the relays are open, no DC current flows to ground, but the open-relay capacitors will charge. This parasitic capacitance per pin is quite small ( $< 10$  pF/pin) and varies among HBM simulators. Since each floating pin is placed in parallel, the parasitic capacitance grows as the number of supply pins connected to the power plane increases. This tester parasitic capacitance is in parallel with the test board capacitance and slows down the HBM peak current rise time on Terminal B and reduces the HBM peak currents. All relay matrix HBM simulators have this property.

The impact on HBM test results is difficult to determine as it depends on the sensitivity of the ESD circuits of the supply pins to slow di/dt rise times. For some designs and equipment, the HBM levels may not be affected at all, or they may either increase or decrease. If failure levels are lower than expected, the best option is to retest the supply pins on a 2-pin manual tester. If the 2-pin HBM levels are much higher, then the open-relay capacitance is probably causing the lower HBM failure levels. In some cases, tester channels can be isolated by adding insulators or removing pogo pins from the HBM tester. This effectively “floats” the parallel supply pins. If there is a known problem for a given package, then special test fixture boards can be designed that connect only one supply pin from the socket to the HBM simulator. This modified test fixture board does not wire the floating pins to the HBM simulator, so these pins cannot charge up the open-relay capacitors.

### **C.5 Test to Determine if an HBM Simulator is an N-channel Low-Parasitic Simulator**

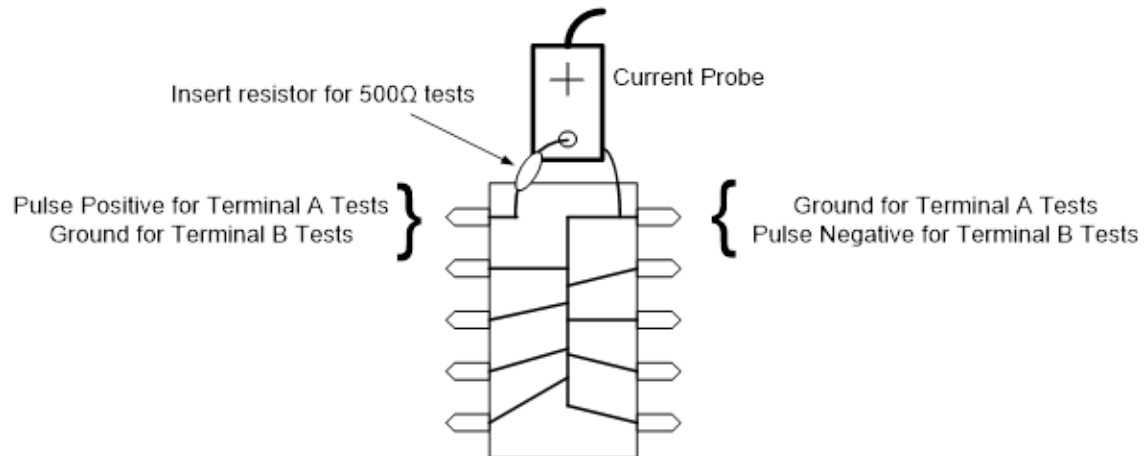
This section describes a test to determine whether a tester can reverse Terminals A and B and produce sufficiently similar waveforms on a DUT that connects N channels.

Prepare a shorting test device using a package compatible with a socket, test fixture, or probes of the simulator under consideration (see Figure 14). Short N pins of the shorting test device together (interconnect with metal) leaving one or more pins free. Add a wire, conforming to shorting load in Section 4.1.3.a, to the shorting test device that passes through a current probe, which meets the requirements of Section 4.1.2. Connect one end of the wire to an unconnected pin of the shorting test device and the other end to the group of N shorted pins. The positive side of the current probe should be connected toward the single pin.

Insert the shorting test device into the HBM tester under consideration. Apply a positive 1000-volt pulse (tester Terminal A) to the single pin with the ground return (Terminal B) connected to any single pin of the connected group. Record this current waveform with an oscilloscope (see Section 4.1.1) and label this waveform as ‘Short Terminal A Current’. Reverse the Terminal A and B connections and pulse the pin of the connected group (now connected to Terminal A) with a negative 1000-volt pulse with the single pin grounded (Terminal B). Record this current waveform as ‘Short Terminal B Current’.

Replace the load with a 500-ohm resistor (conforming to 500-ohm evaluation load in Section 4.1.3.b) and pulse and record 1000-volt 500-ohm waveforms as done with the shorting load to obtain 500-ohm Terminal A current and 500-ohm Terminal B current. Determine the waveform parameters of the recorded waveforms as described in Section 5.2.3.

If all waveform parameters of Table 1 for a short-circuit test load and 500-ohm test load are met by the recorded waveforms, then the tester meets the requirements of a low-parasitic simulator for testing DUTs with up to N pins simultaneously connected to the simulator, as used in this standard.

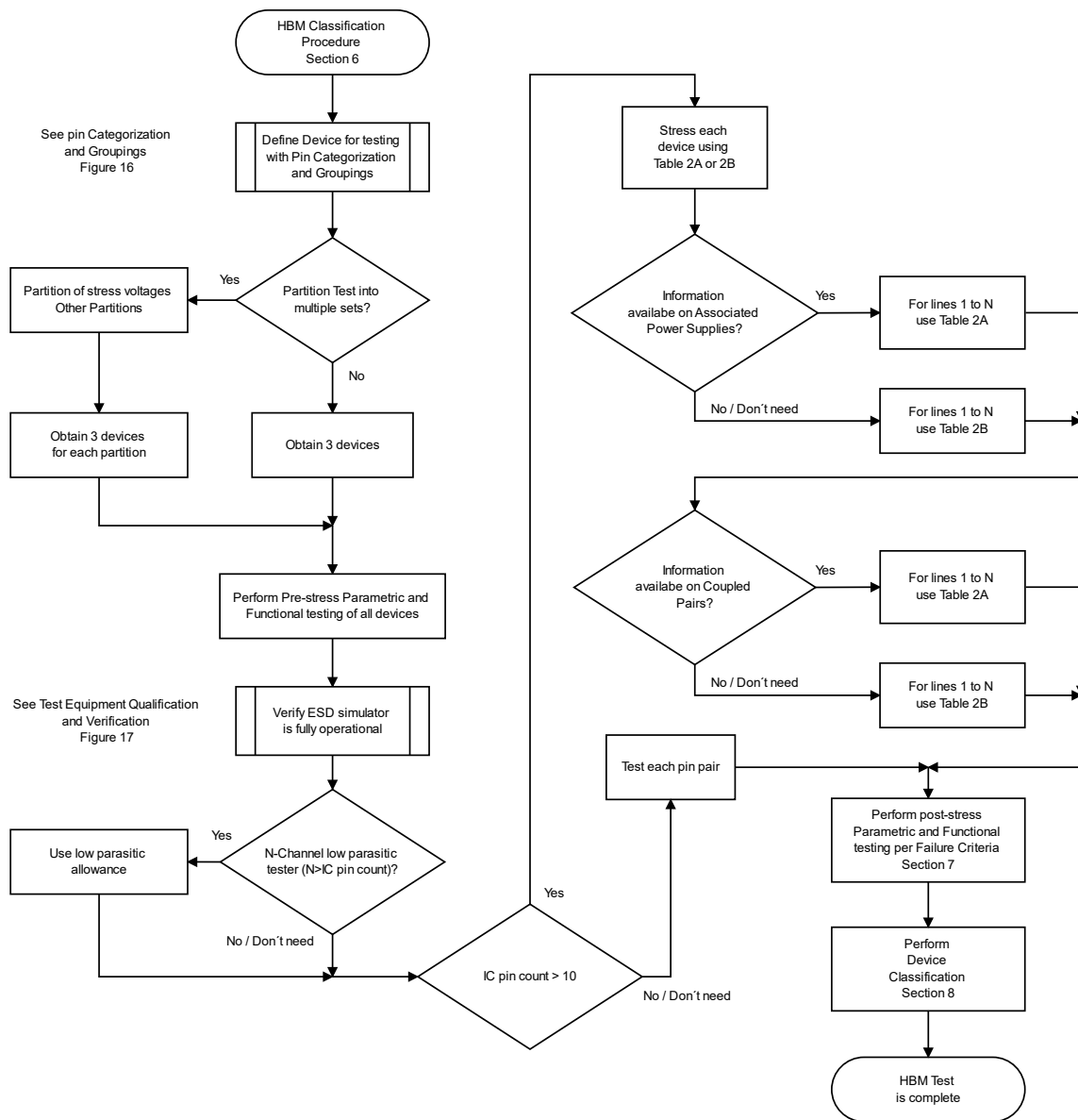


**Figure 14: Diagram of a 10-Pin Shorting Test Device Showing Current Probe**

**NOTE:** The current probe is shown with a 500-ohm test load (to be replaced with shorting load for short test), connected between pin 1 and the shorted group of pins 2 through 10. Pin 1 of this shorting test device is pulsed positive when connected to the tester for a Terminal A test and grounded when for Terminal B tests. Any pin of the connected group can be grounded for Terminal A tests and pulsed negative for Terminal B tests. It is suggested to keep the current probe at the grounded terminal to avoid probe damage.

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## ANNEX D (INFORMATIVE) – HBM TEST METHOD FLOW CHART (PAGE 1 OF 3)



**Figure 15: HBM Classification Procedure**



## ANNEX D (INFORMATIVE) – HBM TEST METHOD FLOW CHART (PAGE 2 OF 3)

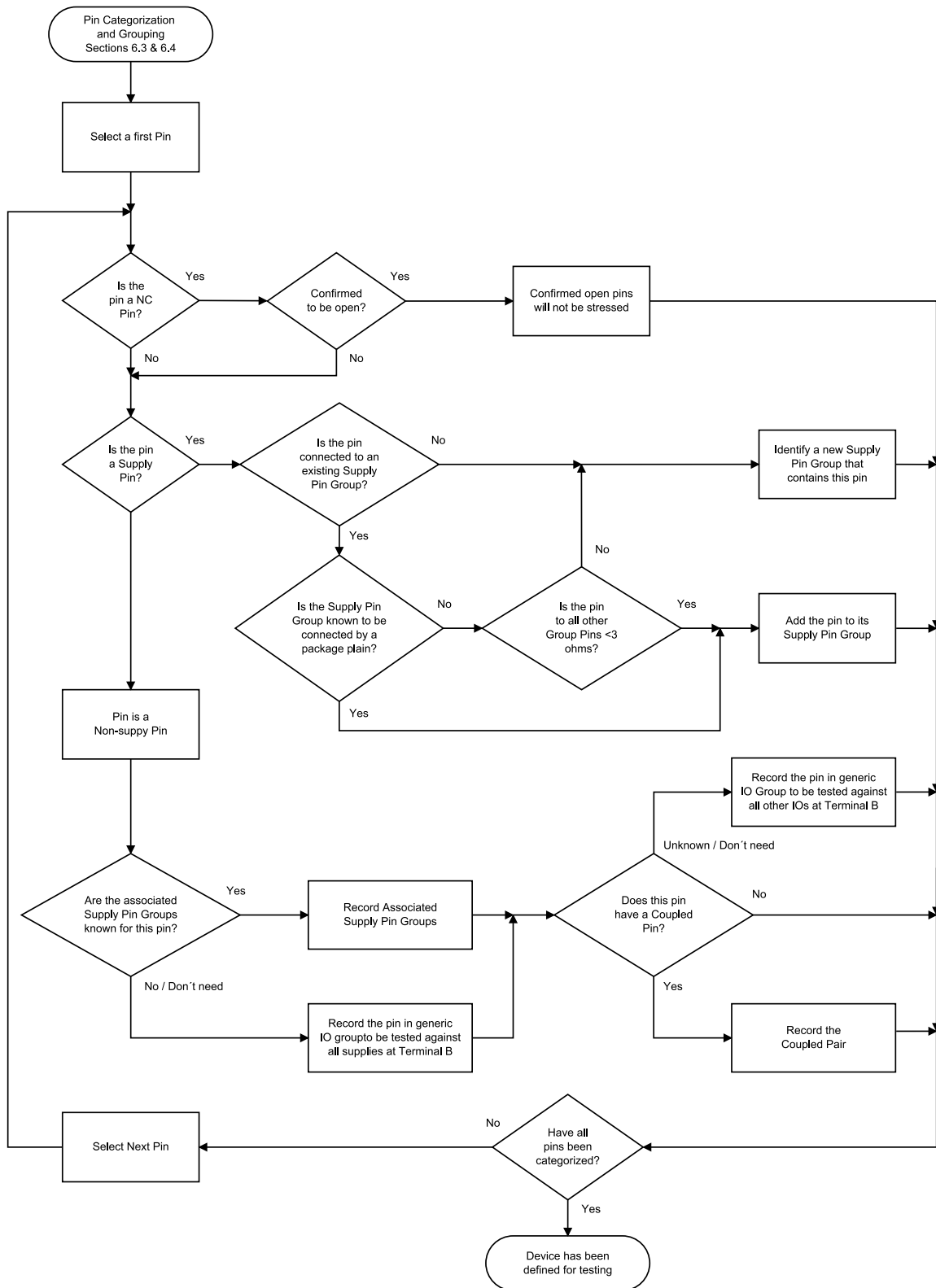
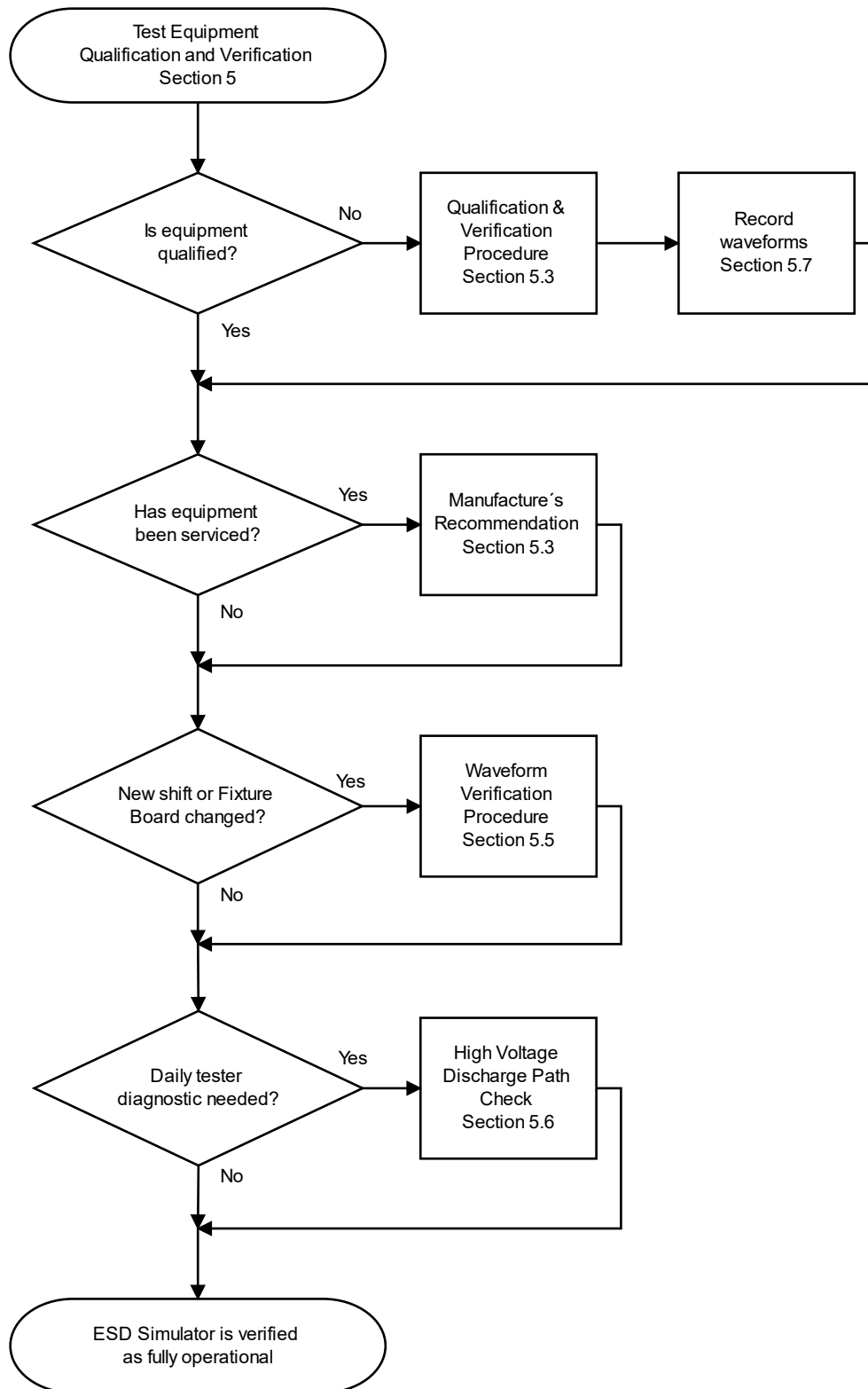


Figure 16: Pin Categorization and Groupings

## ANNEX D (INFORMATIVE) - HBM TEST METHOD FLOW CHART (PAGE 3 OF 3)

*Figure 17: Test Equipment Qualification and Verification*

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(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2023)

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## **ANNEX E (INFORMATIVE) – FAILURE WINDOW DETECTION TESTING METHODS**

As noted in Section 6.2, it is possible, though uncommon, for failure windows to exist below the withstand threshold. When prior experience or knowledge of the technology and the protection elements suggest that this is possible, testing at intermediate voltages is recommended, although not required, to ensure that these windows do not exist on a device. Because the upper and lower bounds of these windows can theoretically be as small as the resolution of the tester, there are practical limits to the voltage levels chosen for low voltage testing. The amount of time and number of units required to complete failure window testing can become quite large if many levels are chosen, and the device has a large number of power supplies and I/O pins.

The selection of voltages and methodology for detecting failure windows depends on the degree of prior characterization and knowledge of the withstand threshold for the device pins. This annex summarizes procedures that can be used if desired to sample at lower voltages and includes an option that allows the re-use of previously stressed parts while minimizing the potential impact of stress hardening due to testing at lower voltages.

### **E.1 Combined Withstand Threshold Method and Window Search**

This method determines the HBM withstand threshold and provides a degree of assurance that there are no failure windows below the HBM withstand threshold. Starting at the lowest voltage level in Table 1, one or more devices should be tested. If the device(s) pass at this voltage, testing should be repeated at the next Table 1 level. The use of fresh devices at each level is preferred but not required. Testing should proceed upwards in Table 1 to a pre-determined (expected passing) higher level in Table 1. If failures are observed below a passing level, there is a failure window. If less than three units were tested at the highest passing level below the failure window, one or two additional devices shall be tested and pass to meet the requirement of three passing devices for the HBM withstand threshold. Finer voltage steps than in Table 1 may be used for a more precise determination of the withstand threshold, increased assurance of the absence of failure windows, and more precise boundaries of any failure windows that are observed.

### **E.2 Failure Window Detection with a Known Withstand Threshold**

This method involves devices with a known withstand threshold level or failure threshold as determined from the test procedure described in Section 6.2 when testing was not performed at all voltage levels. In this case, failure window detection testing involves testing downward in voltage, starting with the known withstand threshold. With this method, units can be re-used based on the premise that working downward in voltage should minimize concerns about stress hardening. Fresh units can also be used if desired. The goal of this testing approach is to test multiple units at multiple voltage levels below the withstand threshold while testing downwards in voltage. One of the main advantages of this method is that it reduces the number of units consumed which is important if the supply of parts is limited or the cost of the parts is very high.

Starting at a voltage below the prior starting voltage, but not less than 50% of that voltage, one device is tested. If the device passes testing at this voltage level, voltage is decremented downward by  $\leq 50\%$  of the prior level, and the testing is repeated (on prior tested passing units or fresh units) until the lowest Table 1 voltage (or less) is achieved. If the first tested device passes each of these voltage levels, additional devices can be stressed at these same voltages or at staggered values between the first set of values to evaluate more low voltage levels. As an example of staggered increments for a device passing 1-kilovolt HBM on three prior units, one of the devices could be tested at 500 volts, 250 volts, and 125 volts, while a second device could be tested at 600 volts, 300 volts, and 150 volts, and a third device at 700 volts, 350 volts, and 175 volts. When starting at higher voltages (for example, 2 kilovolts), the method results in more sampling voltages. If no valid failures are detected at these lower voltages, low voltage testing can be considered complete. If failures are detected at lower voltages, the voltage range of the failure voltage window may be characterized by finer voltage increments.

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2023)

**ANNEX F (INFORMATIVE) - BIBLIOGRAPHY**

MIL-STD-883L, Test Methods and Procedures for Microelectronics: Method 3015.9 Electrostatic Discharge Sensitivity Classification.

MIL-STD-750F w/CHANGE 2, Test Methods for Semiconductor Devices: Method 1020.5: Electrostatic Discharge Sensitivity Classification.

ANSI/ESD STM5.1-2007, ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) Component Level - **Decommissioned**

JESD22 - A114F, December 2008, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) - **Decommissioned**

(This annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2023)

## **ANNEX G (INFORMATIVE) - REVISION HISTORY FOR ANSI/ESDA/JEDEC JS-001**

### **G.1 2011 Version**

This document contains significant changes to the HBM stress methods. Although the new allowances are optional, they may be preferred over the legacy method in many cases. The major changes in the standard are:

- Allowance for non-supply pins to stress to a limited number of supply pin groups (associated non-supply pins).
- Allowance for non-supply to non-supply (that is, I/O to I/O) stress to be limited to a finite number of 2 pin pairs (coupled non-supply pin pairs).
- Explicit allowance for HBM stress using 2 pin HBM testers for die only shorted supply groups.

Minor changes include:

- Supply to supply stress may be done using only a single polarity to overcome the relay matrix capacitance tester artifact.
- “Shorted non-supply pins” connected at the package level or share a common bond pad, do not need to be stressed and may be left unselected during all stresses.
- Stressing products with non-relay testers are recognized and may eliminate redundant stress combinations during stress.

### **G.1.1 Summary by Section**

**1.0 Scope and Purpose** - No changes.

**2.0 Referenced Documents** - No changes.

**3.0 Definitions** - New definitions added for an associated non-supply pin, coupled non-supply pin pair, non-socket tester, socketed tester, non-supply pins, supply pin(s), and two-pin tester. Updated the definitions of human body model (HBM) ESD and no connect pins.

**4.0 Apparatus and Required Equipment** - Only minor changes to this section as outlined below:

4.1.2 Current Transducer (Inductive Current Probe) - added clause (f) for measurement of the decay constant and related note to assist in the selection of transducer.

4.1.3 Evaluation Loads - Updated clause (a) taking into consideration non-socketed testers.

4.2.1 HBM Test Equipment Parasitic Properties - Added the last sentence for two-pin testers and non-socketed testers.

**5.0 Stress Test Equipment Qualification and Routine Verification** - This section was completely rewritten.

5.2.1 Reference Pin Pair Determination - changed second paragraph from “It is recommended that on non-positive clamp fixtures, feedthrough test point pads be added on these paths. These test points should be added as close as possible to the socket(s)” with “It is strongly recommended that on non-positive clamp fixtures, feedthrough test point pads be added on these paths, to allow connection of either the shorting wire or 500-ohm load resistor during waveform verification measurements. These test points should be added as close as possible to the socket(s), and if the test fixture board uses more than one pulse generator, multiple feedthrough test points should be added for each pulse generator’s longest and shortest paths”.

5.2.2.1 Short-Circuit Current Waveform - added a note below clause (b). Added clause (c) for non-socketed testers.

5.2.2.2 500-ohm Load Current Waveform - added clause (a) for socketed testers and clause (b) for non-socketed testers.

5.2.3.1 Short-Circuit Waveform - added the last sentence “A graphical technique for determining  $I_{ps}$  and  $I_R$  is described in Section 5.2.3.3 and Figure 4.”

Added Section 5.2.3.3 defining maximum ringing current.

5.2.4 High-Voltage Discharge Path Test - added the first sentence "This test is only required for relay-based testers". Changed "grounds" into "current return paths".

5.3.1.1 Test Fixture Board, Socket, and Pins for Socketed Testers Only - added "for socketed testers only" in the title.

5.3.1.2 Short-Circuit Waveform Capture - split clause (a) into two different procedures for socketed and non-socketed testers.

5.3.1.3 500-Ohm Load Waveform Capture - split clause (a) into two different procedures for socketed and non-socketed testers.

5.4 Test Fixture Board Qualification for Socketed Testers - added "for socketed testers" in the title.

Table 1 - added first optional row for 125-volt level.

5.5.1 Standard Routine Waveform Check Description - added sentence "For non-socketed testers the procedure of Section 5.2.2.1(c) is used".

5.6.1 Relay-Matrix Testers - moved the content of Section 5.6 into Section 5.6.1. Changed "grounding paths" into "current return paths". Removed the sentence "Use the tester manufacturer's recommended procedure".

5.6.2 Non-Relay Testers - added section.

**6.0 Classification Procedure** - This section was completely rewritten and reorganized.

6.2 Devices for each voltage level - all references to Table 1 changed to Table 3. Added note "It is recommended to verify continuity between device pins and the socket after inserting devices to be tested. Leakage measurements or curve tracing may be used". Added note "References to Table 2 in this section refer to the use of either Table 2A or Table 2B". Added last sentence "It is permitted to partition testing of devices among different testers as long as all testers are qualified (per 5.3) and all pin combinations of Table 2 are tested with at least one sample of three devices".

6.3 Pin categorization - The section has been completely rewritten and reorganized.

6.4 Pin grouping - new section. The former Section 6.4 (no-connect pins) was moved to Section 6.3.1 and updated.

6.5 Pin stress combinations - new section. The former Section 6.5 (non-supply pins) was moved to Section 6.3.3 and updated. New stress combinations are introduced in the document.

6.6 HBM stressing with a low-parasitic simulator - new section. The former Section 6.6 (Alternative Pin Stress Method for Non-Supply Pins) was moved to Section 6.5 and updated.

**7.0 Failure Criteria** - No changes.

**8.0 Classification Criteria** - Minor changes as referenced below:

Added "A component can be classified based on testing with any HBM simulator that meets all the parameters of Section 4.0. If a component tests to a higher classification level on one HBM simulator than another, it is assigned the higher classification.

NOTE: If different classification levels are seen from multiple testers, it is recommended to investigate further".

Table 3 - Previous classification 0 split into new classifications 0A (< 125 V) and 0B (125 V to < 250 V).

### **G.1.2 Annexes**

**A – HBM Test Method Flow Chart** – The flowchart has been expanded to three pages and provides more detail than the previous revision. Associated non-supply pins and coupled non-supply pins have been included along with guidance on which Table 2 should be followed (Table 2A or 2B).

**B – HBM Test Equipment Parasitic Properties** – Section B.4 on low-parasitic simulators was added.

**C – Example of Testing a Product using Table 2A, 2B, or 2A with two pin HBM Tester** – This annex provides an example of how to stress one product using either Table 2A (new methods), 2B (legacy methods) or 2A with a two pin HBM tester. The concepts of associated non-supply pins, coupled non-supply pin pairs, die-shortened supply pins, and package shortened supply pins are all discussed.

**D – Examples of Coupled Non-Supply Pin Pairs** – Provides guidance, based on pin nomenclature, of non-supply pins that may be coupled non-supply pin pairs.

**E – Historical Bibliography** – Title changed.

**F – Alternative Table for Table 2B** – This is the original Table 2 from the ANSI/ESDA/JEDEC JS-001-2010 revision. This table is equivalent to Table 2B and is valid for stressing devices to the legacy method.

## G.2 2012 Version

1. The note section below Figure 1 has been updated; Note 3 has been modified to instruct the user to see Sections 6.5.1.3 and Section 6.6.
2. Section 6.2 Device Stressing has been modified in the second paragraph. The number of HBM pulses has been changed to “at least 1” for the positive and negative pulses.
3. Above Passivation Layer (APL) new definition was defined and Section 6.4.1.3 was added to explain how to use this new layer.
4. Section 6.5.1 has been updated to require recording of more information about the specific pin combination used and the specific HBM tester settings used to reproduce the test.
5. Section 6.6 has been renumbered to 6.7.
6. A new Section 6.6 has been added that describes a low-parasitic HBM simulator and how this type of simulator can be used. Section 6.6.2 references a new updated Annex B.4 section. This annex section has been rewritten and a new figure 10 has been added. The table of contents and the list of figures has been updated to reflect these changes in the document.

## G.3 2014 Version

1. Section 3.0 – Definitions: New definitions added for cloned non-supply pins, exposed pad, feedthrough, SPL, V1, V2, and VM.
2. Table 1 – Waveform Specification: The Ips values were corrected for minor math errors.
3. Section 6.1.1 – Handling Devices: A precautionary statement was added to use safe handling procedures before during, and after HBM and post parametric testing.
4. Section 6.4.2 – Shorted Non-Supply Pin Groups: The shorted non-supply pins that are connected by metal in a package plane was expanded to include APL layer with less than 1 ohm resistance.
5. Section 6.5.1.4 – Cloned Non-Supply (Cloned I/O) Pin Reduction Sampling Method: This new section was added for Cloned Non-Supply pins.
6. Annex G – Cloned Non-Supply (IO) Sampling Pins Test Method: This new annex was added to explain how to apply the HBM testing of cloned non-supply (IO) pins. Sections 1.0 through 1.7 explain how to determine if the non-supply pins meet the definition of cloned non-supply pins, how to select a statistical sample and how to determine if the selected sample size can obtain a 99% or higher confidence level. If the measured fail voltage levels do not provide a 99% confidence level, then the test procedure cannot be used.

The flow chart describes the test procedure steps required to implement this new test procedure.

## G.4 2017 Version

1. Section 3.0 – Editorial and format changes to definitions.
2. Section 4.1.4 – Added specification for oscilloscope attenuator.

3. Section 5.2.2 – Added note concerning use of an attenuator.
4. Section 5.3.1.2 – Clarified when non-optional and optional voltage level waveform verification is required.
5. Table 1 – Added waveform parameters for 50-volt test level.
6. Section 6.1.1 – Added citations of ESD Control Program Standards.
7. Section 6.2 – Added introduction of failure window concept and reference to new Annex H.
8. Table 3 – Added class 0Z (<50 volts) and changed class 0A (50 volts to <125 volts).
9. Added Informative Annex H – Guidelines for detecting failure windows.

#### **G.5 2022 Version**

1. Scope alignment with ANSI/ESDA/JEDEC JS-002 and new sub-chapter on comparing device and wafer-level testing.
2. Word “component” was removed for alignment with JEDEC terms and definitions.
3. Added or modified definitions for an exposed pad, HBM ESD tester, N-channel low parasitic HBM simulator, pin, terminal, tester channel, and two-channel tester. Two-pin tester definition has been removed.
4. Modification in Sections 4.2.1, Section 6.6, Section 6.7, and Annex C (formerly Annex B) to clarify the designation of and allowances resulting from “low parasitics”. The new designation includes the maximum number of pins of a device that can pass the C.4 test procedure.
5. Minor change to Table 1 (Waveform Specification) and to Tables 2A and 2B (Section 6.5).
6. Revised text in several subsections of Section 6 to clarify the “equivalence” of using Table 2A, Table 2B, and pin-pair stressing.
7. Clarified when pin-pair stressing is required (Section 6.2) and clarified that it is permitted for all devices.
8. Revised text in subsection 6.2 and added Annex B on assigning withstand thresholds to a subset of pins.
9. Clarified statement on partitioning testing among different “qualified” testers (Section 6).
10. Addition of Annex C3: Optional Pre-HBM Current Spike Detection Equipment
11. Eliminated Annexes C and D (designated for a move to ESDA/JEDEC JTR001).